

Design of CMOS Architecture for Small Signal Acquisition

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Abstract

This paper describes a method for reducing the power consumption and chip area of small signal acquisition system. In this proposed system, the digital CMOS technology operates with a low supply voltage of 0.5V. Voltage to Time Converter (VTC) block is used for reducing the delay. Digital to Current Converter (DCC) loop is utilized for performing offset cancellation. The Architecture is implemented in a 250nm CMOS technology. A digital feedback loop is employed to cancel the impact of the dc offset in the circuit, which eliminates the need for coupling capacitors.

Key words: CMOS; VTC; DCC; Power consumption; offset cancellation; delay.

INTRODUCTION

The CMOS transistor is normally used as an amplifier when it is working in the saturation region as it has a low dependence with VDS and a high sensitivity to VGS. Digital circuit is used for reducing the supply voltage and helps to achieve increased speed and reduced power consumption. Low power and low voltage are the two important attributes that is addressed in circuits used for small signal, to achieve a long battery life in implantable gadgets as well as monitoring equipment [1]. Low noise and low power small signal amplifiers capable of amplifying signals in the milli-hertz to kilohertz range while rejecting large dc offsets [2]. Low thermal noise is achieved employing MOSTs biased in the weak/moderate inversion region, whereas chopper stabilization is utilized to shift 1/f noise out of the signal band hereby ensuring overall low noise performance. Resulting amplifier, build in a standard 1.5m CMOS process, passes signals from 0.025 Hz to 7.2 kHz with an input referred noise of 2.2 Vrms and a power dissipation of 80 W while consuming 0.16mm² of chip area [3]. With the advancement of CMOS technology, the supply voltage head-room for analog block of an IC. Although the technology scaling leads to lower power consumption and higher performance in digital circuits; many parameters [such as signal-to-noise ratio (SNR), dynamic range, gain, and so on of the analog parts of an IC are negatively impacted. Therefore, it is desirable to find new architectures, in which more digital techniques are introduced [4]. Eliminating the interferences at the input of the system, before substantial gain is applied, can relax the dynamic range requirements and minimize the supply voltage. This can lead to reduce the overall power consumption and area; this is achieved using mixed signal feedback and digital blocks [4], [5], [6]. Hence, it appears that the use of digital techniques in the implementation of these systems can lead to a better performance and better compatibility with digital CMOS technology.

We have designed a new small signal acquisition system. The circuit is designed in 250nm CMOS technology and operates by a supply voltage of 0.5 V. Using the proposed architecture, the area and power consumption is reduced. In Section II, the architecture of the CMOS small signal system is introduced. In Section III, the proposed offset cancellation block is discussed and the TANNER analysis results are presented. In Section IV details the design of the individual circuit blocks. Simulation results are provided in Section V. Finally, the conclusion is drawn in Section VII.

PROPOSED DIGITAL ARCHITECTURE

The proposed block diagram is shown in Fig. 1(a). In this structure, the processing of the small signal is performed in the time and digital domain. The small signal is directly given to the Voltage-to-time converter VTC block and the signal is converted to time.

The time-to-digital converter is used to convert the time mode signal to digital domain. The proposed digital architecture is shown in Fig. 1(b). It consists of VTC_p and VTC_n, a control logic block, a counter, de-multiplexer, and a digital-to-time converter (DCCs). In this proposed architecture the ac coupling capacitors are removed, and the small signal offset is cancelled via a feedback loop. The technique used for the offset cancellation is described in the section III.

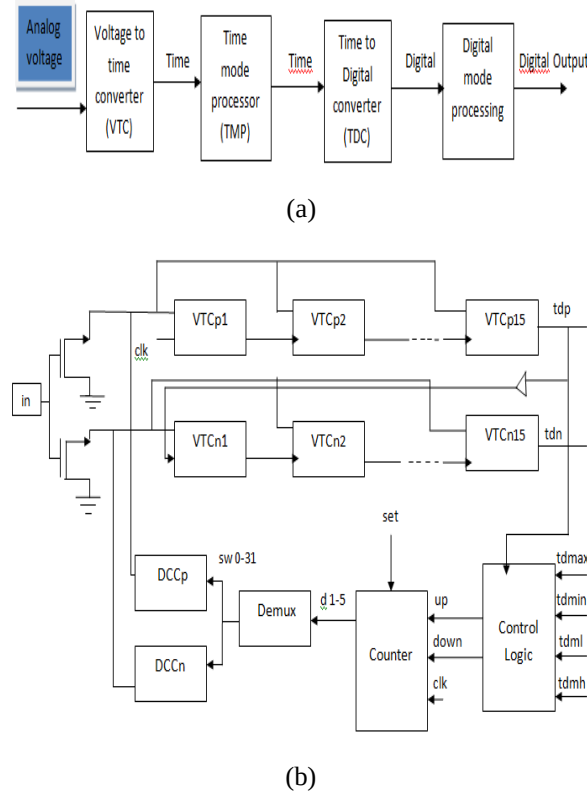


Fig1. (a) Block diagram of the proposed system. (b) Proposed digital architecture.

A. Small Signal

Small signal modeling is a common analysis technique which is used to approximate the behavior of electronic circuits containing nonlinear devices with linear equations. It is applicable to electronic circuits in which the AC signals, the time-varying currents and voltages in the circuit, have a small magnitude compared to the DC bias currents and voltages. A small signal model is an AC equivalent circuit in which the nonlinear circuit elements are replaced by linear elements.

B. Voltage to time converter (VTC)

In the proposed digital architecture, the small signal analog input voltage is converted into time via VTC. The signal information is now in the delay of the clock signal (CLK). The VTC should be designed in such a way that the small amplitude of the input voltage generates a large enough delay, linearly. In order to have time-domain amplification and acceptable SNR, we have used more than 10 stages of positive VTC (VTC_p) and more than 10 stages of negative VTC (VTC_n). The delay versus input voltage of VTC_p and VTC_n are shown in Fig. 2.

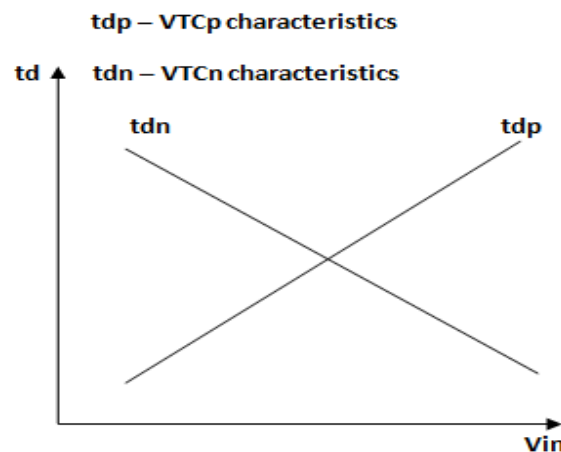


Fig. 2. VTC_n and VTC_p characteristics.

As the input voltage becomes larger, the delay of VTC_p increases, while the delay of VTC_n decreases.

C. Moving Average Filtering

Since, VTCs work with a clock and are broadband compared with the signal bandwidth, not using an anti-aliasing filter before VTCs would lead to out-of-band noise aliasing. The anti-aliasing base signal is a low pass filter signal. A filter that is used to reject high frequency signals before it is sampled to reduce the aliasing. To prevent aliasing and to avoid having an analog filter in the design, we have developed the structure shown in Fig. 3 for converting the voltage to time as well as anti-aliasing filtering. The 15 stages of VTCp and VTCn generate sinc function and is behaving similar to anti-aliasing filter. The clock signal passing through the VTC blocks. When clock is passing through the first stage of VTC, the delay proportional to V_{in} should be generated.

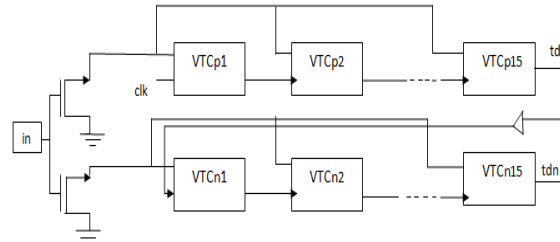


Fig.3. MA-VTC circuit

If the input is small, VTCp block will generate a small delay, $tdp1$ in Fig.4 (e.g. 20% of T_{clk}), and VTCn block will produce a large delay, $tdn1$ in Fig.4 (e.g. 80% of T_{clk}).

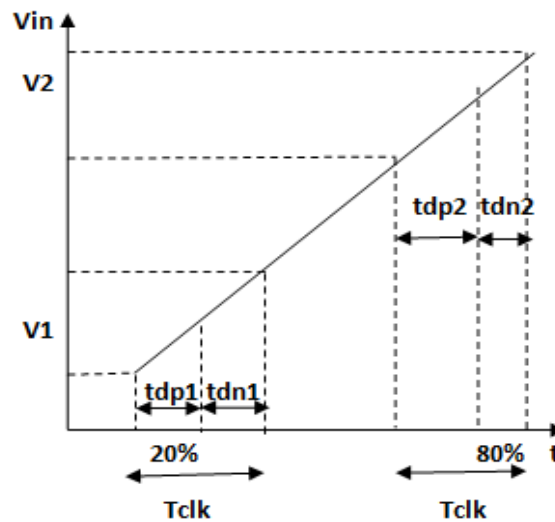


Fig.4. Delays of VTCp and VTCn blocks.

PROPOSED OFFSET CANCELLATION TECHNIQUE

In the proposed architecture, a new offset cancellation technique is used, in which offset cancellation is done in two stages. First, the impact of the offset on the VTCs are eliminated, such that none of the VTCs are saturated. This is achieved by a digital feedback loop and allows the circuit to take the value of the offset to the digital output. In the second stage, the offset can be removed in the digital domain. In our design we have assumed an offset voltage of 50mV.

A. Algorithm

The VTC is linear in the range of -5 to +5mV. This linear region is divided into two regions of R2 and R3. R2 is related to the region for which $tdmh < td < tdm_{max}$ or $tdmin < td < tdm_l$. Similarly, R3 shows the region for which $tdml < td < tdmh$. Besides R2 and R3 regions, R1 represents regions, in which the input is out of predefined linear range 5mV, of the VTC.

B. Architecture

The block diagram is shown in Fig. 5. The proposed architecture contains VTCs, control logic circuit, 5 bit counter, 5-32 demultiplexer, and DCCs. The VTC block is mainly used for reduce the delay and power consumption. DCC feedback loop for eliminate the offset cancellation. The digital feedback loop brings back the delay to region R3 and the impact of the process variations is cancelled.

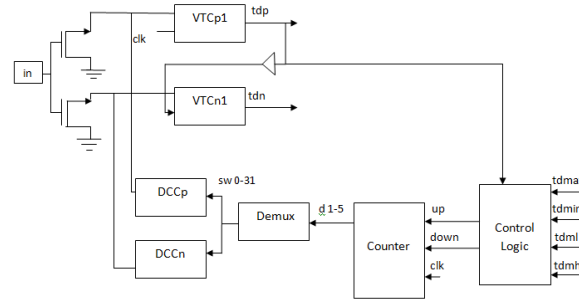


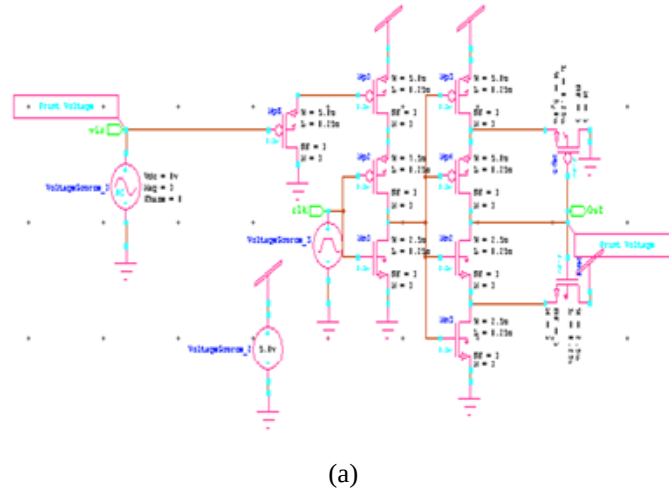
Fig.5. Offset cancellation block diagram

CIRCUIT DESIGN

The proposed digital architecture is implemented in the 250nm CMOS technology. The supply voltage is 0.5V, and the circuits are designed to operate in sub-threshold region to reduce the power consumption.

A. VTC circuit

The VTC block consists of current starved inverter and Schmitt trigger. In the current starved circuit, the rise time of the inverter is controlled by V_{in} through transistor M1. Transistor M0 is a weak minimum size transistor used to allow an alternative circuit path when transistor M1 is off (i.e. when the values of V_{in} is close to the supply voltage). In Tfall current starved circuit, the fall time of the inverter is controlled by V_{in} through transistor M1. Transistor N0 is a weak minimum size transistor used to allow an alternative circuit path when transistor M1 is off (i.e. when the value of V_{in} is less than transistor M1 threshold voltage).

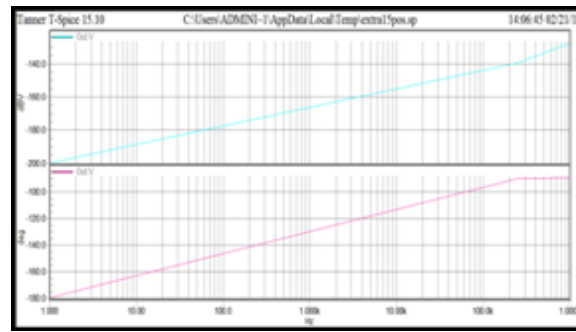


The Schmitt triggers are bi-stable networks that are widely used to enhance the immunity of a circuit to noise and disturbances. It is good as noise rejecter. Schmitt trigger make use of waves, therefore it is widely used for converting analog signals into digital signals. Schmitt trigger diagram is shown in Fig.6. Voltage is applied to the input both M7 and M6 are in OFF condition while M4 and M5 are in ON condition and the output at high logic level. When the input reaches to threshold voltage of M7 transistor then M7 will be on. While M6 remains OFF and at this time output will be high M9 will be ON, so M7 try to pulls up this node to voltage VDD, so transistor M6 stays the output to high logic level, now when the input rises up to threshold voltage of M6 then output switches to low logic level. The difference between the V_{IH} and V_{IL} is referred as HYSTERESIS voltage. Fig.7 shows the VTCs simulation result. This refer to an extra amount of voltage added to low logic level at output or subtracted to high logic level

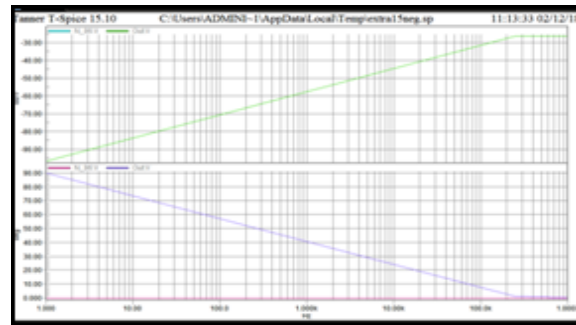
$$tdp = 10^{-6}(+176V_{in} + 8.2) \quad (1)$$

$$tdn = 10^{-6}(-176V_{in} + 8.5). \quad (2)$$

The error between (1) and (2) and the curves obtained from simulations are shown in Fig. 8. When the input voltage varies from -5 to +5 mV, the delay changes by 1.76 us, hence, VTCp and VTCn have a gain of +176 and -176 us/V, respectively. The maximum power consumption at the frequency of 57.8 kHz is 78.26 nW for VTCp and 56.92 nW for VTCn.



(a)



(b)

Fig.7.(a) Delay of the VTCp from simulation. (b) Delay of the VTCn from simulation.

C. PSRR Enhancement Circuit

In the VTCp circuit, we need improve the power supply rejection ratio (PSRR). When the input voltage is given to the VTCp circuit, power supply noise leads to change in V_{sg1} . So the current of M1 should be vary, which leads to change the delay of the system and reduces the PSRR of the proposed architecture. To solve this problem, we have used the PSRR enhancement circuit Fig.9. In this circuit, current variations of transistor M1 due to supply noise is compensated with transistor Mc4 and a current mirror circuit. Current mirror circuit of Mc1-Mc3 prepares the needed current of the block D, which is constant with respect to supply noise.

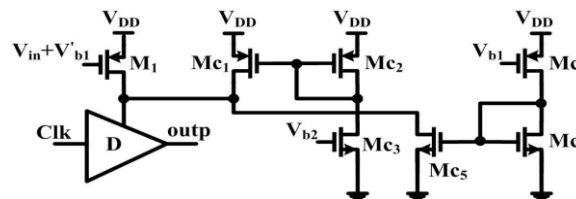
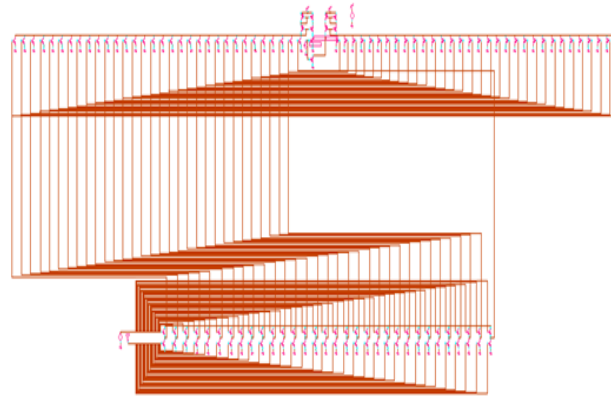


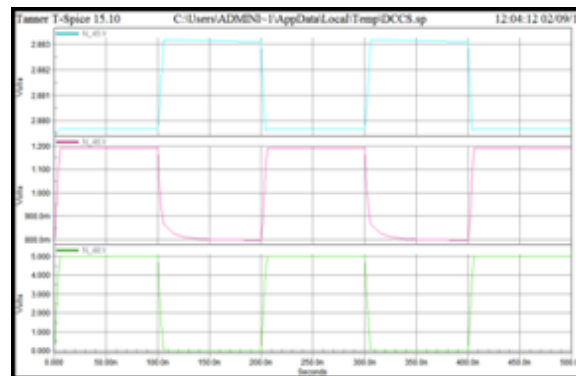
Fig.9. Schematic of the PSRR enhancement circuit.

D. DCCs circuit

The output of the 32-bit de-multiplexer (SW0 to SW31) is given to the DCC blocks. The DCC circuit is shown in Fig.10. In this DCC block the lower circuit generates the gate voltages required for the reference current generator in the upper circuit. The current produced by transistors M_p and M_n to generate the two voltages V_{inp} and V_{inn} . These voltages are applied to the VTCp and VTCn blocks.



(a)



(b)

Fig. 10.(a) DCCs circuit. (b) Transient response of DCCs

E. Control Logic

The control logic is implemented by D flip-flops and are more power and area efficient compared with the analog voltage comparators. Fig.11 shown the control logic block. The outputs of the control logic circuit are the UP and DOWN signals, which control the up/down counter in the offset cancellation block. The counter in our design is implemented by NAND gates and JK flip-flops.

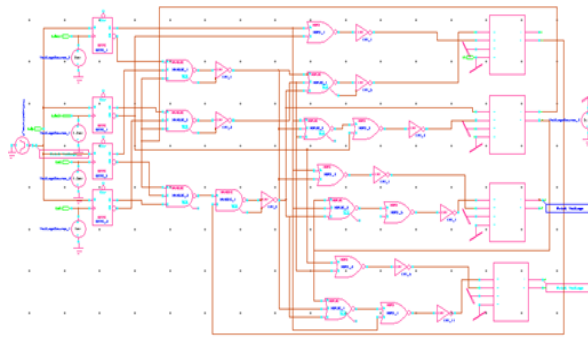


Fig.11. Control logic circuit

SIMULATION RESULTS

The proposed architecture is implemented in 250 nm CMOS technology. The AC analysis of VTC blocks should be shown in Fig.12(a). Output of the VTCp should be linear and output of the VTCn should be non-linear. 5-bit counter block output is UP or DOWN. When the de-multiplexer output should be high the DCC switches are go to ON state. DCCs output V_{inp} and V_{inn} are

feedback of the VTCp and VTCn blocks. The VTC gain is defined as the ratio delay variation at the output of the VTC blocks and the input voltage range.

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