ADVANCES in NATURAL and APPLIED SCIENCES

ISSN: 1995-0772
EISSN: 1998-1090
2016 March 10(3): pages 152-160

Published BY **AENSI Publication**
http://www.aensiweb.com/ANAS
Open Access Journal

Development of Switched Capacitor based Single Phase Multilevel Inverter for Isolated Applications

[1]S. Yasmin Taj, [2]M.Yamuna and [3]Dr. H. Habeebullah Sait

[1]PG Student, P.S.R. Engineering College, Sivakasi, India.
[2]Assistant Professor, P.S.R. Engineering College, Sivakasi, India.
[3]Assistant Professor, Anna University, BIT Campus, Tiruchirapalli, India.

Received 25 January 2016; Accepted 28 March 2016; Available 10 April 2016

Address For Correspondence:
S. Yasmin Taj, PG Student, P.S.R. Engineering College, Sivakasi, India..
E-mail: taj_yasmin@yahoo.in

ABSTRACT

This paper presents a single-phase nine-level inverter for stand-alone Photo-voltaic systems with a pulse width modulated (PWM) control scheme. The proposed nine-level inverter comprises a single-phase conventional H-bridge inverter, three bidirectional switches and four capacitor voltage dividers. The control signal generated by using four sinusoidal reference signals that are compared with one triangular carrier signals for controlling the switches of the inverter. The inverter is capable of generating the nine levels of output voltage of more fundamental RMS output voltage with less amount of THD. The proposed nine-level inverter has been verified through MATLAB simulation results.

KEYWORDS: Multilevel inverter, photovoltaic (PV) system, pulsewidth-modulated (PWM), Total Harmonic Distortion (THD).

INTRODUCTION

Due to increase in energy demand and rapid depletion of non-renewable resources, power electronic researchers are focusing in the field of alternative energy sources. The renewable energy source predictable to efficiently contribute the humanity energy for almost 1billion years. The renewable energy sources would also reduces the costs of operation and environmental pollution caused by burning of fossil fuels. Photo-voltaic generation system is one of the most popular renewable energy sources. The generated energy from the photovoltaic system is used in stand-alone application and it can be delivered to the power network.

The multilevel inverter concept is the kind of alteration of two-level inverter. The general structure consists of four switches found in the single-phase inverter is to create a sinusoidal voltage from several levels of voltage, typically obtained from capacitor voltage sources. The main motivation for such inverter is that the current is shared among these multiple switches, allowing a high inverter power rating than the individual switch VA rating. Otherwise it allows harmonics. As the number of level increases, the synthesized output waveform, a staircase wave like, approaches a desired waveform with decreasing harmonic distortion, approaching zero as the number of level increases.

Several types of multilevel inverter topologies, which have been reported from high power inverter system manufacturers. The most commonly used topologies are diode clamped, flying capacitor or multicell, cascaded H-bridge and modified H-bridge multilevel inverter topologies. These three topologies employ different mechanism to produce the required output. The diode clamped multilevel inverter uses clamping diodes along with series connected capacitor whereas, in flying capacitor type, floating capacitors are used to facilitate clamp

the output voltage and in cascaded type is the simply series connection of H-bridges. The main concept of this diode clamped multilevel inverter is to use diodes and provides multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The drawback of diode clamped multilevel inverter is difficult, because of quadratic relation between number of diode and number of level especially, when number of level is higher and also it becomes stressful to maintain charging and discharging cycle. This trouble can be overcome by increasing the switches, diodes and capacitors. Due to the capacitor balancing issues, these are limited to the three levels. In flying capacitor type, flying capacitors are required as a substitute of clamping diodes. The drawback of flying capacitor multilevel inverter is the output is half of the input dc voltage and it also has the switching redundancy within phase to balance the flying capacitors. The cascaded H-bridge multilevel inverter consists of H-bridge cells and each cell can provide the three different voltages like zero, positive dc and negative dc voltages. This type of topology requires less number of components as compared with diode clamped and flying capacitor type inverters. Separate dc source should be required to the every H-bridge cell. Due to the multiple dc sources, unequal voltage may be appeared.

This paper proposes the development of novel modified single phase single source nine level inverter with novel pulse width modulated scheme are discussed in section II.

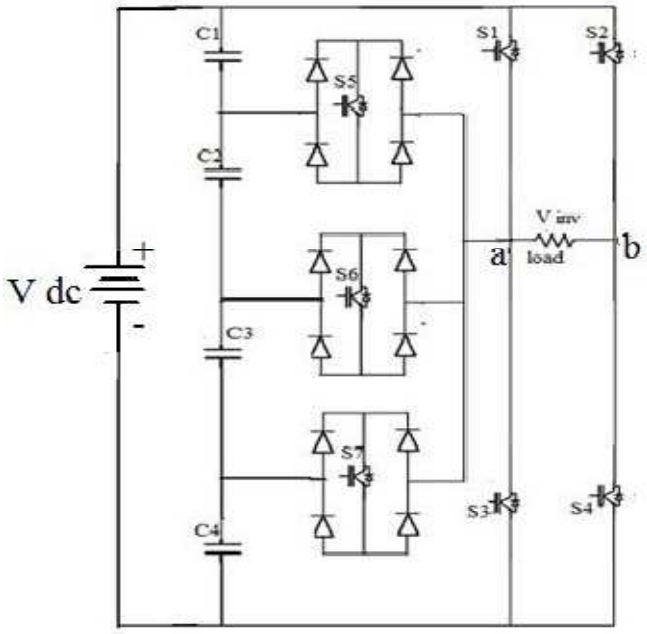


Fig. 1: Power circuit diagram of proposed nine-level inverter.

Proposed nine levels Inverter Topology:

The nine level single-phase single dc sourced inverter consists of single-phase conventional H-bridge inverter, three bidirectional switches and four capacitor voltage dividers C_1, C_2, C_3 and C_4. The H-bridge inverter topology has lot of advantageous over diode clamped and flying capacitor multilevel inverter topologies, it requires less number of components for inverters of the same number of levels and so its overall weight and price is less. The power generated by the multilevel inverter is to be delivered to the isolated load. Nine output voltage levels can be produced by proposed switching of the multilevel inverter from the single dc supply voltage. The output voltage levels are V_{dc}, $3V_{dc}/4$, $2V_{dc}/4$,$V_{dc}/4$, 0, $-V_{dc}/4$,$-2V_{dc}/4$,$-3V_{dc}/4$,$-V_{dc}$.

The conducting modes are expressed as follows:

Mode 1: $0 < \omega t < \theta_1$ and $\theta_6 < \omega t < \pi$
Mode 2: $\theta_1 < \omega t < \theta_2$ and $\theta_5 < \omega t < \theta_6$
Mode 3: $\theta_2 < \omega t < \theta_3$ and $\theta_4 < \omega t < \theta_5$
Mode 4: $\theta_3 < \omega t < \theta_4$
Mode 5: $\pi < \omega t < \theta_7$ and $\theta_{12} < \omega t < 2\pi$
Mode 6: $\theta_7 < \omega t < \theta_8$ and $\theta_{11} < \omega t < \theta_{12}$
Mode 7: $\theta_8 < \omega t < \theta_9$ and $\theta_{10} < \omega t < \theta_{11}$
Mode 8: $\theta_9 < \omega t < \theta_{10}$.

The various levels of output voltage part nine level inverter were generated as follows.

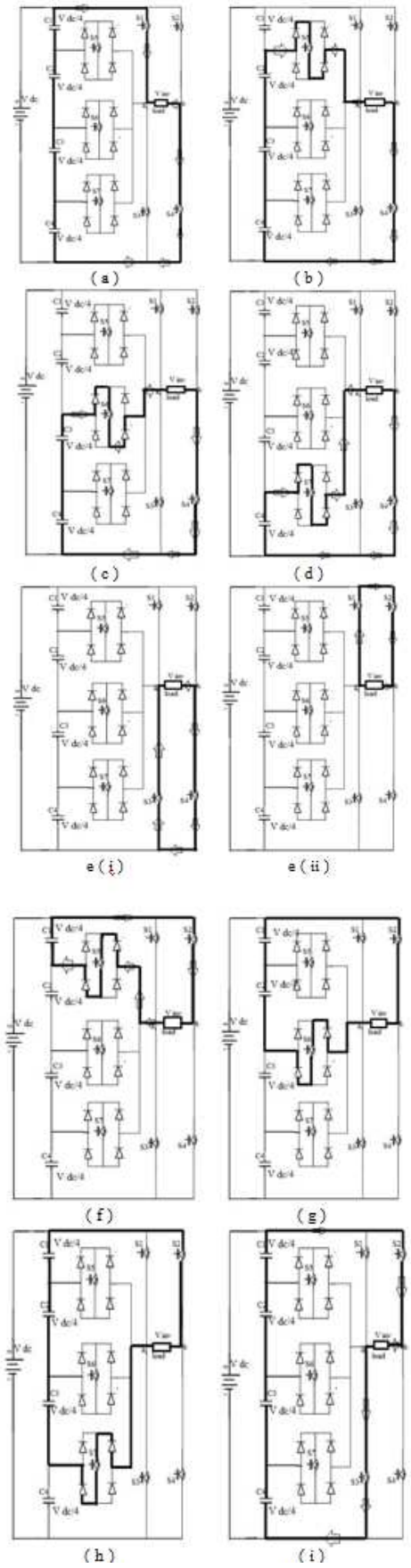


Fig. 2: Different modes of operation of proposed nine level inverter (a)$V_{ab}=V_{dc}$, (b)$V_{ab}=3V_{dc}/4$, (c)$V_{ab}=2V_{dc}/4$, (d)$V_{ab}=V_{dc}/4$, e (i) and (ii) $V_{ab}=0V_{dc}$, (f) $V_{ab}= -V_{dc}/4$,(g)$V_{ab}= -2V_{dc}/4$, (h)$V_{ab}= -3V_{dc}/4$, (i)$V_{ab}= -V_{dc}$.

Table 1: Output voltage according to the switches ON-OFF condition for nine-level inverter.

Inverter output voltage	Switching State combination						
	S_1	S_2	S_3	S_4	S_5	S_6	S_7
V_{dc}	1	0	0	1	0	0	0
$3V_{dc}/4$	0	0	0	1	1	0	0
$2V_{dc}/4$	0	0	0	1	0	1	0
$V_{dc}/4$	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
	1	1	0	0	0	0	0
$-V_{dc}/4$	0	1	0	0	1	0	0
$-2V_{dc}/4$	0	1	0	0	0	1	0
$-3V_{dc}/4$	0	1	0	0	0	0	1
$-V_{dc}$	0	1	1	0	0	0	0

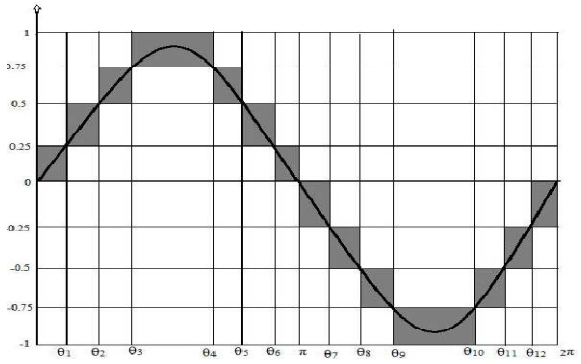


Fig. 3: Output voltage and switching angles for nine level inverter.

Mode 1: Maximum Positive Output Voltage (+V_{dc}):

In this mode of operation, the switches S_1 and S_4 conduct. During this period, the current flows from switch S_1, load and S_4. When switch S_1 is ON, the load positive terminal connecting to V_{dc} and when switch S_4 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is $+V_{dc}$. Figure 3(a) shows the current path of this mode.

Mode 2: Three-Fourth Positive Output Voltage (+3V_{dc} /4):

In this mode, the bidirectional switch S_5 and S_4 conducts. During this period, the current flows from bidirectional switch S_5, load and switch S_4. When the bidirectional switch S_5 is ON, the load positive terminal connecting to V_{dc} and when switch S_4 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is (+3V_{dc} /4). Figure 3(b) shows the current path of this mode.

Mode 3: Two-Fourth Positive Output Voltage (+2V_{dc} /4):

In this mode, the bidirectional switch S_6 and S_4 conducts. During this period, the current flows from bidirectional switch S_6, load and switch S_4. When the bidirectional switch S_6 is ON, the load positive terminal connecting to V_{dc} and when switch S_4 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is (+2V_{dc} /4). Figure 3(c) shows the current path of this mode.

Mode 4: One-Fourth Positive Output Voltage (+V_{dc} /4):

In this mode, the bidirectional switch S_7 and S_4 conducts. During this period, the current flows from bidirectional switch S_7, load and switch S_4. When the bidirectional switch S_7 is ON, the load positive terminal connecting to V_{dc} and when switch S_4 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is (+V_{dc} /4). Figure 3(d) shows the current path of this mode.

Mode 5: One-Fourth Negative Output Voltage(-V_{dc} /4):

In this mode, the bidirectional switch S_5 and S_2 conducts. During this period, the current flows from bidirectional switch S_5, load and switch S_2. When the bidirectional switch S_5 is ON, the load positive terminal and when switch S_2 is ON, the load negative terminal connecting to V_{dc}. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is (-V_{dc} /4). Figure 3(f) shows the current path of this mode.

Mode 6: Two-Fourth Negative Output Voltage (-2V_{dc} /4):

In this mode, the bidirectional switch S_6 and S_2 conducts. During this period, the current flows from bidirectional switch S_6, load and switch S_2. When the bidirectional switch S_6 is ON, the load positive terminal and when switch S_2 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is (-2V_{dc} /4). Figure 3(g) shows the current path of this mode.

Mode 7: Three-Fourth Negative Output Voltage (-3V_{dc} /4):

In this mode, the bidirectional switch S_7 and S_2 conducts. During this period, the current flows from bidirectional switch S_7, load and switch S_2. When the bidirectional switch S_7 is ON, the load positive terminal and when switch S_2 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is (-3V_{dc} /4). Figure 3(h) shows the current path of this mode.

Mode 8: Maximum Negative Output Voltage (-V_{dc}):

In this mode, the switches S_2 and S_3 conduct. During this period, the current flows from switch S_2, load and S_3. When switch S_2 is ON, the load negative terminal connecting to V_{dc} and when switch S_3 is ON, the load positive terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal is -V_{dc}. Figure 3(i) shows the current path of this mode.

III Development of PWM Scheme:

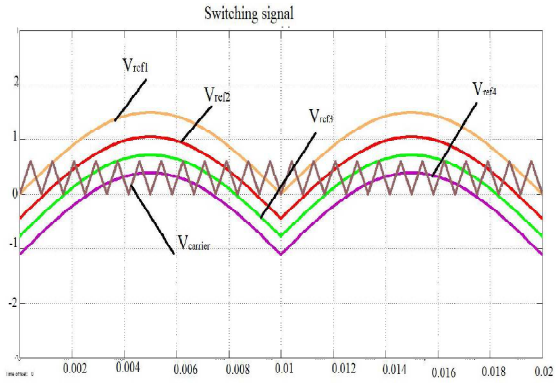
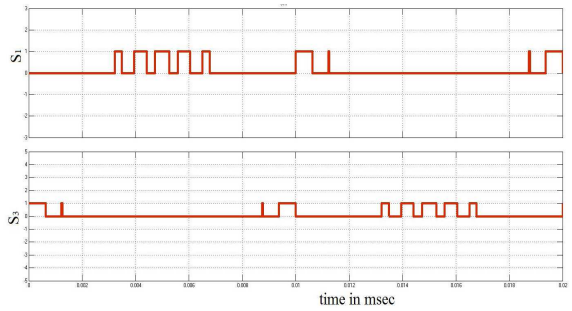


Fig. 4: Single carrier and four sinusoidal reference signal.

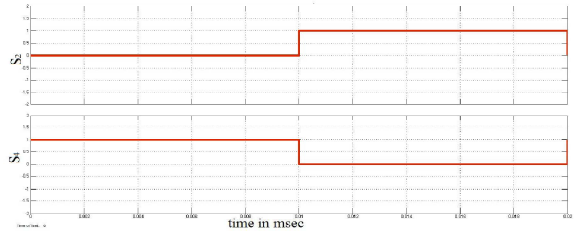
The PWM modulation scheme which utilizes four sinusoidal reference signal has fundamental frequency with single triangular carrier signal of high frequency. Fig.4 and fig.5 shows the generation of switching pattern to control and produce nine level inverter output voltages. To generate the PWM signals for the switches of the inverter, a novel PWM modulation technique was developed. Four sinusoidal reference signals (V_{ref1}, $V_{ref2,}$ V_{ref3} and V_{ref4}) were compared with the carrier signal. If the amplitude of V_{ref1} has exceeded the peak amplitude value of $V_{carrier}$, then the amplitude of V_{ref2} was compared with $V_{carrier}$ until the reference signal amplitude has the exceeded the peak amplitude of $V_{carrier}$. Then the amplitude of V_{ref3} would be compared with carrier signal until it reached zero. Once V_{ref3} had attained zero, V_{ref2} would be compared with $V_{carrier}$ until it reached zero. Then the amplitude of V_{ref4} would be compared with carrier signal until it reached zero. Once V_{ref4} had attained zero, V_{ref1} would be compared with $V_{carrier}$ until it reached zero. Switches S_1, S_3, S5, $S_{6\ and}$ S_7 would be conducting at the rate of frequency of the carrier signal, whereas S_2 and S_4 would operate at equivalent to the fundamental frequency. The modified inverter operated into eight conducting modes for one cycle of the fundamental frequency.

The phase angle value varies with modulation index M_a. Theoretically, the modulation index for a single reference signal and a single carrier signal is defined to be $M_a = A_m / A_{c.}$ Whereas the modulation index for a dual-reference signal and a single carrier signal is defined to be $M_a = A_m / 2A_{c,}$ the seven level PWM inverter utilizes three-reference signal and single carrier signal is defined to be $M_a = A_m / 3A_c$, since the proposed nine level inverter utilizes four-reference signal and single carrier signal is defined to be $M_a = A_m /4A_{c.}$ where A_c represents the peak-to-peak value of carrier signal and A_m represents the peak value of voltage reference signal V_{ref}. The phase angle displacement for the modulation index value is less than 0.25 is defined to be $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta_5 = \theta_6 = \pi/2$; $\theta 7 = \theta_8 = \theta_9 = \theta_{10} = \theta_{11} = \theta_{12} = 3\pi/2$. Since the phase angle displacement for the modulation index value is between 0.25 and 0.5 is defined to be $\theta_1 = \sin^{-1}(Ac/Am)$; $\theta_3 = \theta_4 = \pi/2$; $\theta_6 = \pi - \theta_1$; $\theta_7 = \pi +$

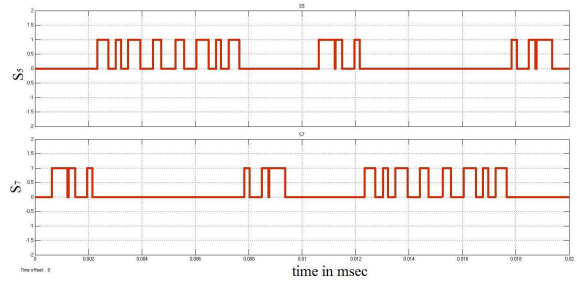
θ_1 ; $\theta_9 = \theta_{10} = 3\pi/2$; $\theta_{12} = 2\pi - \theta_1$. If the modulation index value is more than 0.75, the phase angle displacement is $\theta_1 = \sin^{-1}(Ac/Am)$; $\theta_2 = \sin^{-1}(2Ac/Am)$; $\theta_3 = \sin^{-1}(3Ac/Am)$; $\theta_5 = \pi - \theta_2$; $\theta_7 = \pi + \theta_1$; $\theta_8 = \pi + \theta_2$; $\theta_{11} = 2\pi - \theta_2$; $\theta_{12} = 2\pi - \theta_1$. Only the lower reference signal (Vref4) is compared with the triangular carrier signal for Ma value that is equal to, or less than 0.25. The inverter's performance is like that of the conventional full-bridge three-level PWM inverter. However, only the V_{ref2} and V_{ref3} reference signals are compared with the triangular carrier signal for M_a value is between 0.25 and 0.5, for that the output voltage consists of five dc-voltage levels. The V_{ref3} and V_{ref4} reference signals are compared with the triangular carrier signal for M_a value is between 0.5 and 0.75. The output voltage consists of seven dc-voltage levels. The nine level output voltage to be produced for the modulation index value is more than 0.75. Four sinusoidal reference signals have to be compared with the single triangular carrier signal to produce the switching signals for control the switches of the inverter.



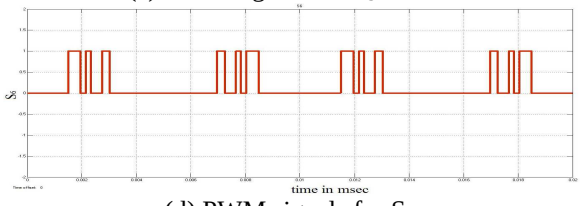
(a) PWM signals for S_1 and S_3



(b) PWM signals for S_2 and S_4



(c) PWM signals for S_5 and S_7



(d) PWM signals for S_6

Fig. 5: Detail switching signal for the single-phase nine level inverter.

IV Investigation of Proposed Inverter:

The proposed single phase nine level inverter with PWM technique simulink model is shown in fig.6. For nine level inverter one H-bridge, three diode embedded bidirectional switches and four capacitor voltage dividers are needed.

Fig.7 shows the PWM switching generation of nine level inverter. Four sinusoidal reference signal with base frequency should be compared with high frequency triangular carrier signal. The one leg of the H-bridge switches is operated in fundamental frequency, whereas the other leg switches are operated at high switching frequency.

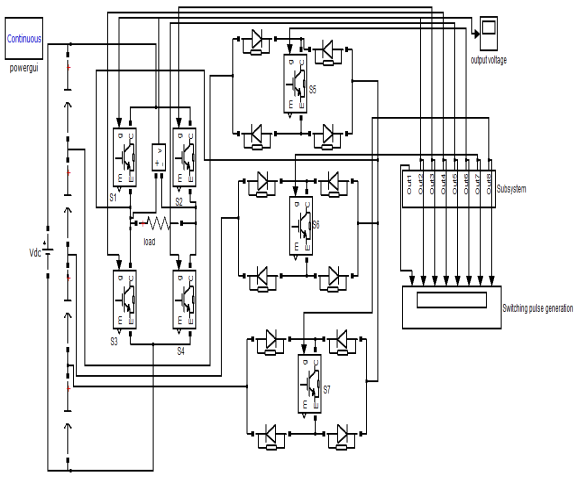


Fig. 6: Simulation of nine-level inverter.

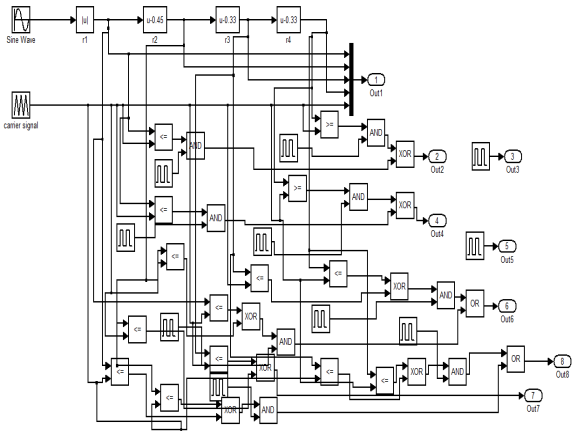


Fig. 7: Simulation of PWM switching generation.

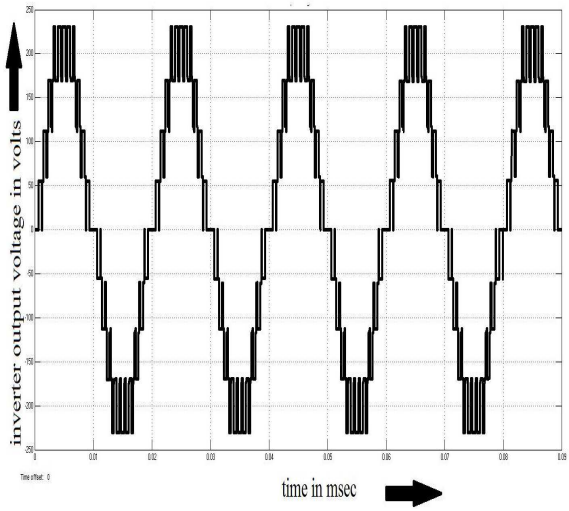


Fig. 8: Output voltage for Proposed nine-level inverter.

The simulation result of inverter output voltage (V_{inv}) for nine-level inverter is shown in Fig.8. The inverter output voltage consists of nine levels (V_{dc}, $V_{dc}/4$, $2V_{dc}/4$, $3V_{dc}/4$, 0, $-V_{dc}/4$, $-2V_{dc}/4$, $-3V_{dc}/4$, $-V_{dc}$). The output voltage of the inverter can be controlled by varying the modulation index of the inverter. The level of the output voltage changes with range of modulation index, which is discussed earlier.

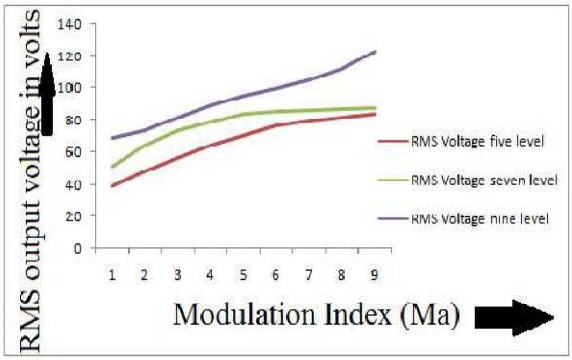


Fig. 9: Comparison of modulation index and RMS output voltage.

Fig.9 shows the graphical representation of comparison between Modulation index and RMS output voltage. From this representation, the value of RMS output voltage of nine level inverter is higher than the single-phase five-level and seven-level inverter. So that, nine level inverter provides better performance.

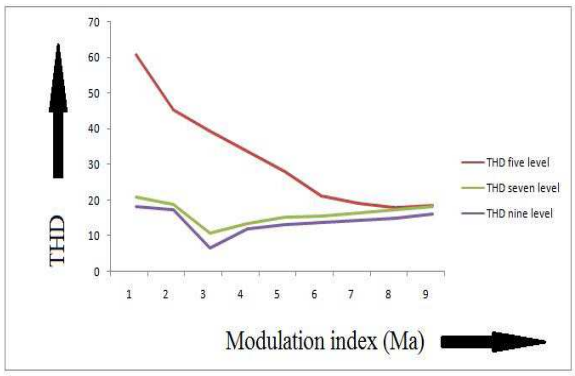


Fig. 10: Comparison of modulation index and THD.

Fig.10 shows the graphical representation of comparison between Modulation index and Total Harmonics Distortion (THD) value. From this representation, the THD value of nine level inverter is decreased as compared to the five level and seven level inverter for the same value of Modulation index.

Conclusion:

This paper carried out the development of nine level inverter for stand-alone Photovoltaic system for isolated applications. A novel PWM switching scheme has been developed and implemented for the nine level inverter. From this simulation studies, it is inform that, the performance of single-phase single DC sourced switched capacitored nine-level inverter provides improved THD with high value of fundamental rms output voltage for various values of modulation index. The performance of nine level inverter is compared with five and seven level inverter in terms of RMS output voltage and THD values. It concludes that, the nine level inverter is an attractive solution for stand-alone renewable energy systems.

REFERENCES

1. Babaei, E., S. Laali, Z. Batat, 2015. "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind.Electron.*, 62(2): 922-929.
2. Mokhberdoran, A., A. Ajami, 2014. "Symmetric and Asymmetric design and implementation of new cascaded multilevel inverter topology", *IEEE Trans. Power Electron.*, 29(12): 6712-6724.
3. Kangarlu, M.F., E. Babaei, 2013. "A Generalized Cascaded Multilevel Inverter Using Series connection of submultilvel Inverters", *IEEE Transaction on Power Electron.*, 28(2): 625-636.
4. Selvaraj, J., N.A. Rahim, 2009. "Multilevel inverter for grid-connected PV system employing digital PI controller," *IEEE Trans. Ind. Electron.*, 56(1): 149–158.
5. Rahim, N.A., J. Selvaraj, 2010. "Multi-string five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, 57(6): 2111–2121.
6. Nasrudin Abd Rahim, Jeyaraj Selvaraj, Krismadinata Chaniago, 2011. "Single-phase seven-level grid-

connected inverter for photovoltaic system" *IEEE trans. Ind. electron.*, 58(6): 2435-2443.
7. Rodriguez, J., S. Bernet, B. Wu, J.O. Pontt and S. Kouro, 2007."Multi-level voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, 54(6): 2930–2945.
8. Kjaer, S.B., J.K. Pedersen and F. Blaabjerg, 2005. "A review of single-phase grid connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, 41(5): 1292–1306.
9. Peng, F.Z., 2001. "A generalized multilevel inverter topology with self volt-age balancing," *IEEE Trans. Ind. Appl.*, 37(2): 611–617.
10. Cheng, Y., C. Qian, M.L. Crow, S. Pekarek and S. Atcitty, 2006. "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, 53(5): 1512– 1521.
11. Tolbert, L.M., F.Z. Peng, T. Cunnyngham and J.N. Chiasson, 2002. "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, 49(5): 1058–1064.
12. Agelidis, V.G., D.M. Baker, W.B. Lawrance and C.V. Nayar, 1997. "A multilevel PWM inverter topology for photovoltaic applications," in *Proc. IEEE ISIE*, Guimäes, Portugal, 589–594.
13. Park, S.J., F.S. Kang, M.H. Lee and C.U. Kim, 2003. "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, 18(3): 831–843.