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Cascaded Multilevel Inverter with Series Connection of H-Bridge units

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ABSTRACT

cascaded multilevel inverter with series connections of H-bridge units is proposed. In order to generate all voltage levels (even and odd) at the output, nine different are proposed to determine the magnitudes of dc voltage sources. This topology is able to increase the number of output voltage levels by using a lower number of power electronic devices such as switches the number of different voltage amplitudes of the used sources is decreased the different approaches to the construction of multilevel inverter are explained and compared. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed High power quality, lower harmonic components, better electromagnetic consistence, lower dv/dt, and lower switching losses the proposed topology with its presented algorithms in generating all voltage levels have been verified by using the experimental results of a 49-level single-phase inverter MATLAB/SIMULINK.

KEYWORDS: cascaded multilevel inverter, total harmonic distortion (THD), lower harmonic components, 49-level single-phase inverter.

INTRODUCTION

The single-phase cascaded multilevel inverter based on H-bridge units is proposed. In order to generate all voltage levels (even and odd) at the output, nine different algorithms are proposed to determine the magnitudes of dc voltage sources. This topology is able to increase the number of output voltage levels by using a lower number of power electronic devices such as switches the number of different voltage amplitudes of the used sources is decreased the different approaches to the construction of multilevel inverter are explained and compared. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed High power quality, lower harmonic components, better electro magnetic consistence, lower dv/dt, and lower switching losses the proposed topology with its presented algorithms in generating all voltage levels have been verified by using the experimental results of a 49-level single-phase inverter.The multilevel inverters have received much attention because of their considerable advantages such as high power quality, lower harmonic components, better electromagnetic consistence, lower *dv/dt*, and loss

Power electronics inverter are the essential equipment to convert and control the electrical power in the wide range of mille watts to giga watts with the help of semiconductor devices. These inverters are finding increased attention in recent years. Hence, highly efficient power electronic technologies and reliable control strategies are needed to reduce the loss of energy and to improve power quality. High power electronic devices are being used increasingly to control and facilitate flow of electric power while meeting stringent-operating conditions of present heavily loaded networks.

In recent years, numerous industrial applications have begun to demand higher power equipment. Medium voltage motor drives and their applications require medium voltage to megawatt power level. It is hard to connect

a single power semiconductor switch directly to a medium voltage grid. As a result, a multilevel power inverter structure has been introduced as an alternative in high power and medium voltage situations. The main advantage of these inverters is the low number of different voltage amplitudes of the used dc sources. However, the higher number of required insulated gate bipolar transistor (IGBTs), power diodes, and driver circuits in generating a specific output level are their remarkable disadvantages. In order to increase the number of output levels with a lower number of power semiconductor devices, different asymmetric cascaded multilevel inverters have been presented in.

The bidirectional power switches have been used in these topologies. Each bidirectional power switch includes two IGBTs, two power diodes, and one driver circuit if the common emitter configuration is used. Therefore, in these topologies, the installation space and total cost of the inverter increase. As a result, several asymmetric cascaded multilevel inverters have been presented in which the unidirectional switches from the voltage point of view and the bidirectional switches from the current point of view are used in them. Each unidirectional switch consists of an IGBT with an anti parallel diode. Two of these topologies have been presented in Two other algorithms for the H-bridge cascaded multilevel inverter have been also presented in and . Because of the asymmetric topology and used unidirectional switches, it seems that the lower number of power electronic devices is the main advantage of these inverters. However, the main disadvantage of the asymmetric topologies is the lost of modularity, which means the use of a high variety of semiconductor devices.

Multilevel inverters have also emerged as an attractive choice in the field of medium-voltage to high-voltage industrial drive applications, which include motor drives, power distribution, power quality, and power conditioning applications. It is important that the multilevel inverter is introduced as a solution to increase the inverter operating voltage above the voltage limits of classical semiconductors. Using this concept, the power conversion is performed in small voltage steps, resulting in better power quality. These inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating. Additionally, the harmonic content of output waveform decreases significantly as the number of inverter levels increases.

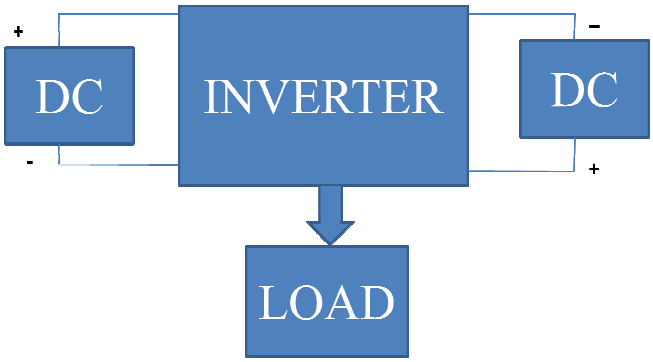

Fig. 1: Block diagram of cascaded multilevel inverter with series connections of h-bride unit.

II. Conventional Cascaded Multilevel Inverter

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975. Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and presented its various advantages in 1997. Since then, the CMI has been utilized in a wide range of applications. With its modularity and flexibility, the CMI shows superiority in high-power applications, the DC source voltage magnitude. In the cascaded multilevel inverter, all the voltage sources are needed to be isolated from one another. Thus for five level inverter, two DC sources are needed. The switching stress can be reduced because of its better switch utilization.

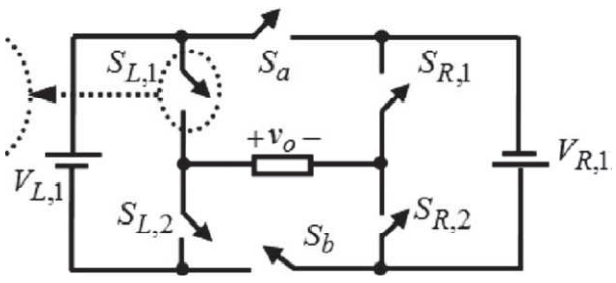

Fig. 2: five level cascaded inverter.

Table 2.1: Switching states for cascaded five-level inverter

State	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	v_o
1	1	0	0	1	0	1	$V_{L,1}$
2	0	1	1	0	0	1	$V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0
	0	1	0	1	0	1	
5	0	1	1	0	1	0	$-V_{L,1}$
6	1	0	0	1	1	0	$-V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}+V_{R,1})$

Table 2.1 shows the generated output voltage levels based on the different switching patterns in the proposed basic unit. In this table, 1 and 0 indicate the on and off states of the switches, respectively. As shown in Table I, this basic unit is able to generate seven levels (three positive levels, three negative levels, and one zero level) at the output. In addition, in each switching pattern, one power switches from each leg (*SL*,1 or *SL*,2), (*SR*,1 or *SR*,2), and *Sa* or are turned on simultaneously. If the magnitudes of the dc voltage sources are equally considered, the proposed inverter can generate five levels at the output. Therefore, in order to generate more numbers of output levels at the output, the magnitude of dc voltage sources have to be selected differently. Therefore, the magnitude of the dc voltage sources is considered as follows.

The other main parameter in calculating the total cost of the inverter is the maximum amount of the blocked voltage by switches. If the values of the blocked voltage by switches are reduced, the total cost of the inverter decreases. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to the values of the blocked voltage by switches *SR*,1 and *SR*,2 are equal to output values.

Proposed Method For Multilevel Inverter With Reduced Number Of Switches:

Multilevel inverters have received more attention for their ability on high-power and medium voltage operation and because of other advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference. These inverters generate a stepped voltage waveform by using a number of dc voltage sources as the input and an appropriate arrangement of different symmetric cascaded multilevel inverters have been presented. The main advantage of all these structures is the low variety of dc voltage sources.

3.1 First method:

If all DC voltage sources in Figure 5.2equal to V_{dc}, the inverter is then known as symmetric multilevel inverter. The number of maximum output voltage steps of the n series basic units can be evaluated by

$N_{step}=n+1$ (1)

The reason for using the term ‘‘maximum” is that it is possible to have an equal value for V_0over different states of the switches. The maximum output voltage is given by:

$V_{o,max} = n \times V_{dc}$ (2)

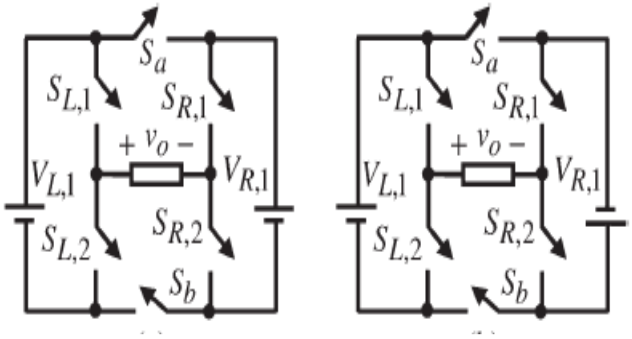

Fig. 3: Basic unit for a multilevel inverter.

3.2 Cascaded basic units:

This topology requires multiple DC sources, in some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. When AC voltage is already available, multiple DC sources can be generated using isolated transformers and rectifiers

Table 3.1: Output voltage 7 level inverter.

OUTPUT VOLTAGES OF THE PROPOSED SEVEN-LEVEL INVERTERS

No.	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	v_o (Fig. 1(a))	v_o (Fig. 1(b))
1	1	0	0	1	0	1	$V_{L,1}$	$V_{L,1}$
2	1	0	0	1	1	0	$V_{R,1}$	$-V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}-V_{R,1}$	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0	0
	0	1	0	1	0	1		
5	0	1	1	0	1	0	$-V_{L,1}$	$-V_{L,1}$
6	0	1	1	0	0	1	$-V_{R,1}$	$V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}-V_{R,1})$	$-(V_{L,1}+V_{R,1})$

The other main parameter in calculating the total cost of the inverter is the maximum amount of the blocked voltage by switches. If the values of the blocked voltage by switches are reduced, the total cost of the inverter decreases. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 2, the values of the blocked voltage by switches *SR*,1 and *SR*,2 are equal to the multi level inverter.

Table 3.2: Values ofV_0 for state of switches.

	Switch states						
State	S_1	S_2	S_3	S_4	S_{2n-1}	S_{2n}	V_0
1	off	On	Off	on	off	on	0
2	on	Off	Off	on	off	on	V_1
3	off	On	On	off	off	on	V_2
4	on	Off	On	off	off	on	V_1+V_2
2^n	On	Off	On	off	on	off	$\sum_{i=1}^{n} V_1$

The overall output voltage equation of the suggested cascaded multilevel inverter is $v_0 = v_{0,1} + v_{0,2} + \cdots + v_{0,n}$. Table 4.2 shows the value of v_0 for state of switches $S_1, S_2 \ldots S_{2-1}, S_{2n}$. As can be seen, 2^n different values can be obtained forv_0.

The main aim of proposing the new cascaded multilevel inverter is to increase the number of output voltage levels by using a lower number of components. In order to investigate the performance of the proposed topology from the number of different voltage amplitudes.

3.3 Second method:

The second method for determination of the magnitudes of DC voltage sources is in binary fashion which gives an exponential increasing in the number of the overall output levels. For n series basic units, with DCvoltage levels varying in binary fashion, the number of maximum output voltage steps and maximum output voltage are calculated by

$$N_{step} = 2^n \quad (3)$$

3.4 Third method:

In the third method, the DC voltage sources in the proposed multilevel inverters are suggested to be chosen according to the following equations:

$$V_1 = V_{dc} \quad (4)$$

$$V_j = 2V_{dc} \text{For j=2, 3, 4…n} \quad (5)$$

The number of maximum output voltage steps can be determined by the following equation:

$$N_{step} = 2^n$$

3.5 Comparison of the suggested structure with conventional cascaded multilevel inverter:

The conventional symmetric cascaded multilevel inverter is indicated by *R*1and the conventional binary asymmetric cascaded multilevel inverter is shown by *R*2. Three other algorithms have been presented for this topology in and which are indicated by *R*3–*R*5, respectively. The main purpose of this project is reduction of the components of the cascaded multilevel inverters. Each switch in the suggested topology is composed of one insulated-gate bipolar transistor (IGBT) and one anti-parallel diode. Also, each switch requires one gate driver as show the output values.

IV. Simulation Diagram:

4.1 5 Level Cascaded H-Bridge Inverter:

The 5 level cascaded H-bridge Multilevel inverter circuit diagram as shown in figure. In this figure 5.1 shows simulation block diagram of 5 level cascaded H-bridge Multilevel inverter.This block diagram one number of cells. this cell four number of switches are used. Basic formula 2N+1 N=number of cell. This topology is 8 number of switches are used. This topology is normal 5 level cascaded H-bridge Multilevel inverter. This block diagram are resistive load are connected

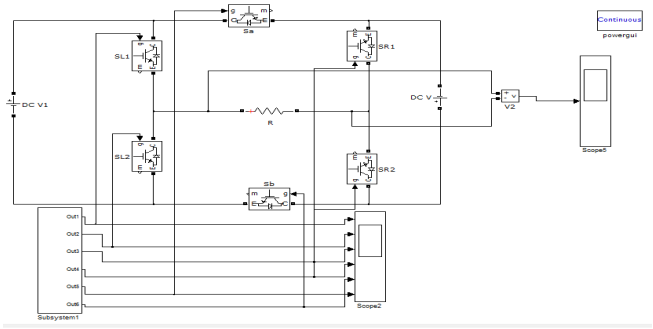

Fig.4: Simulation Block Diagram of 5 Level Cascaded H-Bridge Inverter.

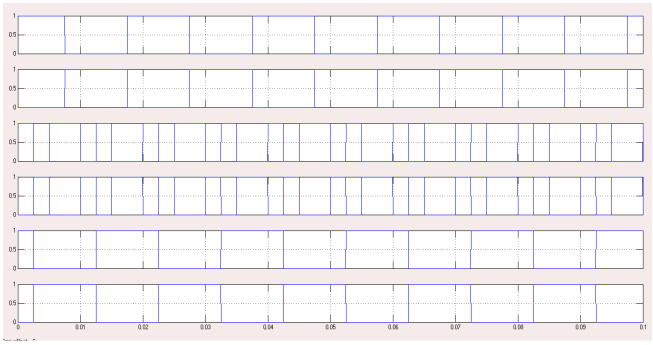

Fig. 5: Gate pulse for proposed method of 5-level.

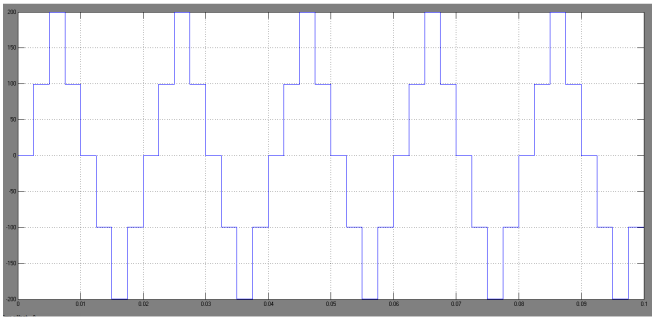

Fig.6: Output Voltage Waveform of 5 Level Cascaded H-Bridge Inverter.

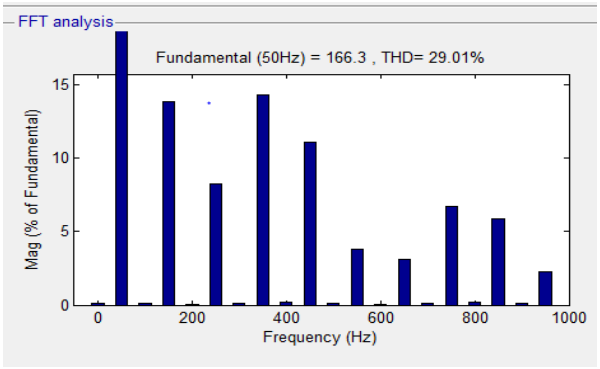

Fig.6: Total Harmonic Distortion In 5 Level.

V. 7 Level Cascaded H-Bridge Inverter:

Seven level inverter is modeled similar to that of the three-level and five-level inverter. The difference here is also the number of carrier signals. Here we are taking six carrier signals. Three of them are applied across the positive half cycle of the modulating signal. Remaining three of them are applied across the negative half cycle of the modulating signal.

5.1 7 Level Sub System:

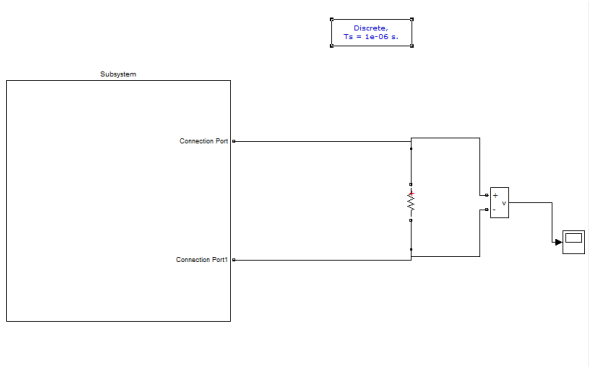

Fig.7: 7level subsystem.

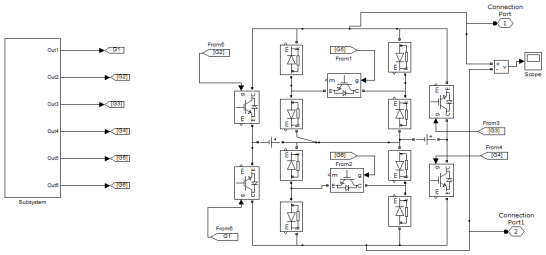

Fig.8: Simulation Block Diagram of 7 Level Cascaded H-Bridge Inveter.

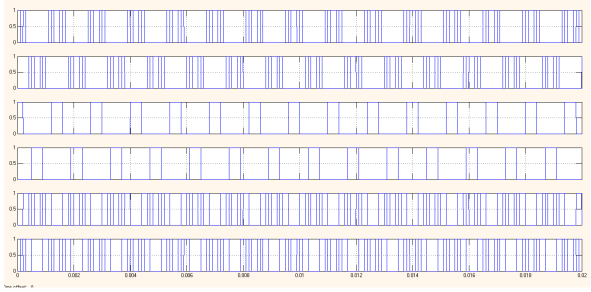

Fig.9: Gate pulse for proposed method of 7-level.

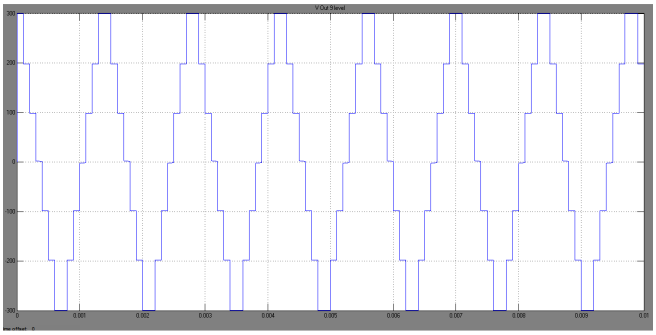

Fig.10: Output Voltage Waveform of 7 Level Cascaded H-Bridge Inverter.

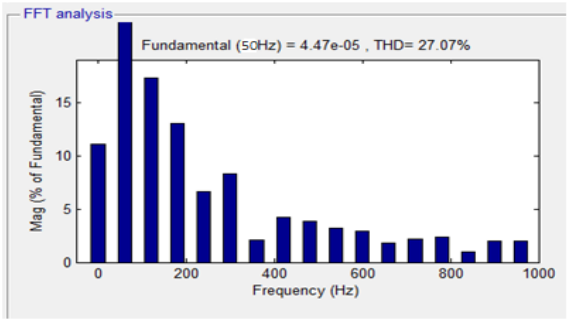

Fig. 5: 9 Total Harmonic Distortion In 7 Level.

VI. 49 Level Cascaded multilevel inverter H-bride inverter.

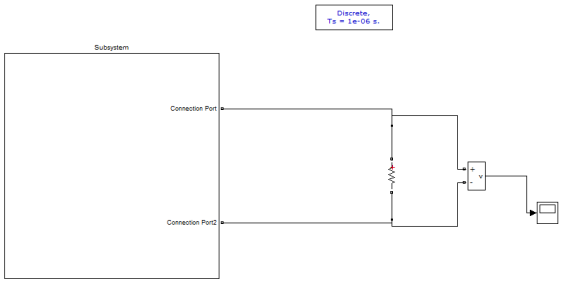

Fig.11: 49 Level subsystem.

6.1 49 level switching functions:

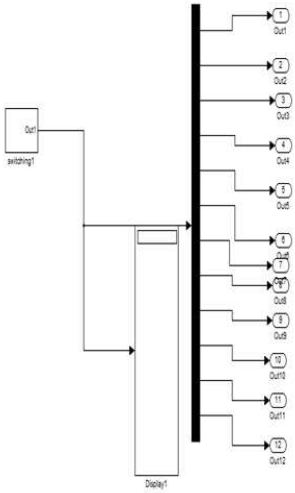

Fig.12: switching functions.

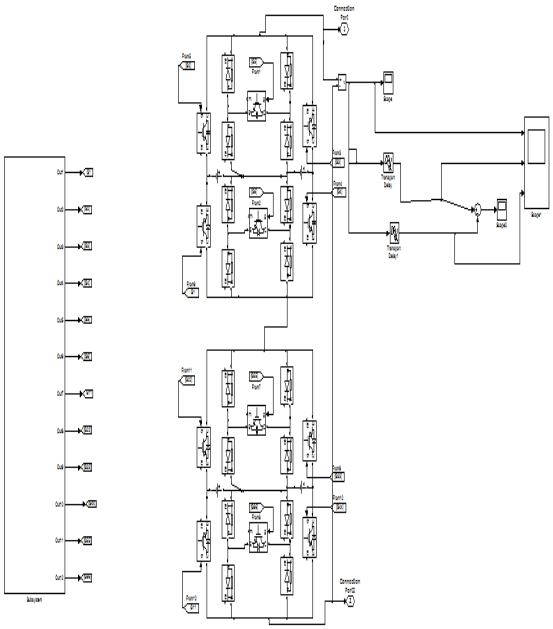

Fig.13: Simulation Block Diagram of 49 Level Cascaded H-Bridge Inverter.

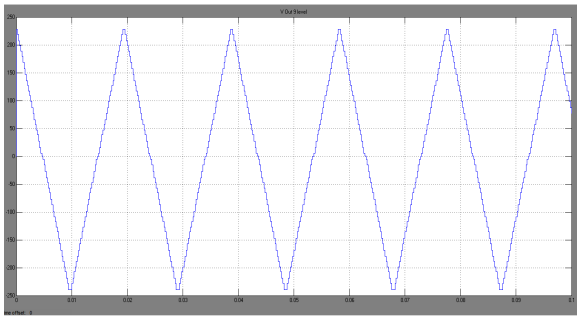

Fig.14: Output Voltage Waveform of 49 Level Cascaded H-Bridge Inverter.

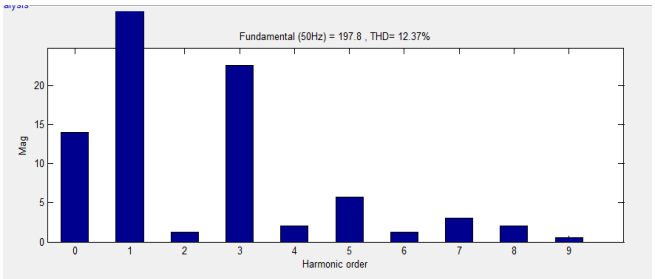

Fig. 15: Total Harmonic Distortion In 49 Level.

Conclusion:

A new configuration of cascaded multilevel inverter has been proposed. The suggested topology needs fewer switches and gate driver circuits with minimum standing voltage on switches for realizing N_{step} for the load. Therefore, the proposed topology results in reduction of installation area and cost and has simplicity of control. When the number of level is increased, the THD is reduced significantly.

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