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# A New Cascaded Multilevel Inverter with Reduced Number of Switches

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## ABSTRACT

A Multilevel Inverter (MLI) is one of the attractive topology for DC to AC conversion. It synthesizes the desired voltage wave shape from several number of DC sources voltage summation. Multilevel Inverter provides unidirectional power flow between on DC sources and load. Due to this, we can get a balanced output voltage with desired frequency. In recent day's Multilevel Inverter can be used for high voltage and high power application and has many advantages like, low switching stress, low total harmonics distortion (THD). This proposes a new topology of cascaded Multilevel Inverter with reduced number of switches compared with an conventional Multilevel Inverter. In this proposed topology, we can generate high number of level with reduced number of switching devices. Therefore with less number of switches, there will be reduction in gate drive circuitry and THD value. Due to this period, very few switches will be conducting for specific intervals of time. A comparison is made for the topologies for different level and an effective reduction in THD has been observed for the circuits with less number of switches. The circuits are modelled and simulated with the help of MATLAB/SIMULINK (R2012a).

**KEYWORDS:** Multilevel Inverter (MLI), Total Harmonics Distortion (THD).

## INTRODUCTION

In recent days MLI has drawn large interest in high power industry. They present a latest set of aspects to facilitate and utilized in reactive power compensation. The unique arrangement of multilevel voltage source inverters allow them to achieve high voltages with the low harmonics not including the utilization of transformers or series connected synchronized switching devices. The Diode clamped, Flying capacitor and Cascaded H-bridge inverter are the three main different types of multilevel inverter structures which are used in industrial applications with separate dc sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcome in cascaded H-bridge inverter. Conventional cascaded seven level multilevel inverter require twelve switches and three dc sources separately.

These designs can create power excellence for a given number of semiconductor devices higher than the fundamental topologies alone due to a multiplying effect of the number of levels. Also, some soft switching methods can be applied for different multilevel inverters to reduce the switching loss and to increase efficiency. Babaei *et al* have discussed different multilevel inverter topologies. Advantages of this multilevel method include good power quality, good electro-magnetic compatibility, low switching losses and high voltage capability. Unfortunately, multilevel inverters have some drawbacks. One particular drawback is the great number of power semiconductor switches needed. While low voltage rating switches can be employed in a multilevel inverter, each switch needs an associated gate driver circuit. This may cause the whole system to be more expensive and complex. So, in practical implementation, reducing the switch count and gate driver circuits is of immense interest.

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This paper proposes a new topology for cascaded multilevel inverters with a high number of steps related with a low number of switches and gate driver circuits for switches. In addition, for producing odd level at the output voltages for calculating the required DC voltage sources are proposed. Finally, the simulation results are presented to prove the feasibility of the proposed multilevel inverter topology.

*Existing Topologies:*

*(a) Cascaded H-Bridge Multilevel Inverter:*

The full-bridge topology with four switches is used to produce a three-level square-wave output voltage waveform. The cascaded multilevel inverter consists of series connections of n full-bridge topology. Figure1 shows the configuration of cascaded multilevel inverter.

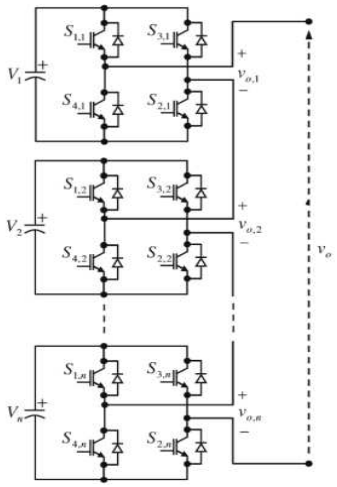

**Fig. 1:** Configuration of Cascaded H-Bridge Multilevel Inverter.

*The whole output voltage of multilevel inverter is given by:*

$V_0 = V_{01}+V_{02}+V_{03}+.....+V_{0n}$

If all DC voltage sources in figure1 equal to $V_{dc}$, the inverter is known as symmetrical multilevel inverter. The actual number of output voltage steps ($N_{step}$) in symmetric multilevel inverter may be related to the number of full bridges (n) by:

$N_{step} = 2n+1$

And the maximum output voltage ($V_{0,max}$) of this n-Cascaded Multilevel Inverter is:

$V_{0,max}) = n \text{ X } V_{dc}$

**Table 1:** Switching requirement for Cascaded H-Bridge Multilevel Inverter.

| Level | Number of switches |
|---|---|
| 5 | 8 |
| 7 | 12 |
| 9 | 16 |
| 11 | 20 |

*(b). Existing Topology 1:*

Although this topology requires several DC sources, in some systems they may be offered through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. When AC voltage is already available, multiple DC sources can be generated using insulated transformers and rectifiers.

*First Method*

If all DC voltage sources in Figure 2 equal to $V_{dc}$ , the inverter is then known as symmetric multilevel inverter. The number of maximum output voltage steps of the n series simple units can be evaluated by:

$N_{step} = n+1$

The reason for using the term ‘‘maximum” is that it is possible to have an equal value for $V_0$ over different states of the switches. The maximum output voltage is given by:

$V_{0,max} = N \text{ x } V_{dc}$

*Second Method:*

The second method for determination of the magnitudes of DC voltage sources is in binary fashion which gives an exponential increasing in the number of the overall output levels. For n series basic units, with DC voltage levels varying in binary fashion, the number of maximum output voltage steps and maximum output voltage are calculated by:

$N_{step} = 2^n$

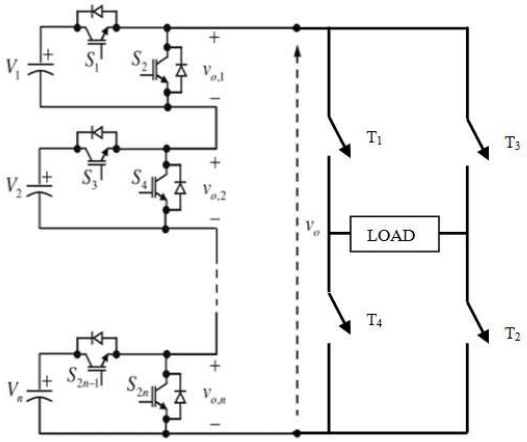


**Fig. 2:** Configuration of Existing Topology 1.

**Table 2:** Switching requirement for existing topology 1.

| Level | Number of switches |
|---|---|
| 5 | 8 |
| 7 | 10 |
| 9 | 12 |
| 11 | 14 |

*(c). Existing Topology 2:*

This topology consists of a series connected set of inverters which are capable of producing a stepped output. No two switches in the same leg conduct at the same time so as to prevent short circuit across the voltage source. Each voltage source is Vdc and thus we can get a maximum voltage 3Vdc. We get 7-level output voltage having Vdc, 2V dc, 3Vdc in positive half cycle, zero level, -Vdc, -2Vdc, -3Vdc in negative half cycle. H-bridge takes care of the positive and negative level voltages. Switches S1 and S2 serve for positive level. S3 and S4 serve for negative level.

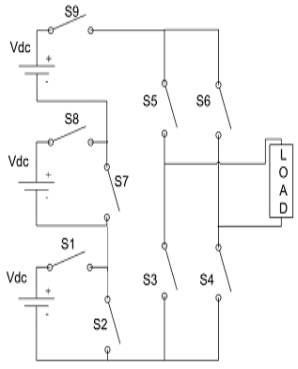


**Fig. 3:** Configuration of 7 level 9 switch topology.

*Proposed topology:*

The proposed topology is simple in design and compared to the existing topologies, it consists of 'n' number of dc sources and 'n' number of switches are required for achieve 'n' number of levels. In compared with an existing topology it offers 'n' number of levels with minimum number of switches. It also have additional features like only three switches conducting at an interval of time. Two switches used for polarity reversal and the remaining switches are used for waveform generation.

**Table 3:** Switching requirement.

| Level | Number of switches |
|---|---|
| 5 | 7 |
| 7 | 9 |
| 9 | 11 |
| 11 | 13 |

The generalized expression for number of dc sources for the proposed topology is given by:

$V = (N-1)/2$

Where N = Number of levels

V = Number of DC sources

The generalized expression for number of levels for the proposed topology is given by:

$N = (2*V) + 1$

Where N = Number of levels

V = Number of DC sources

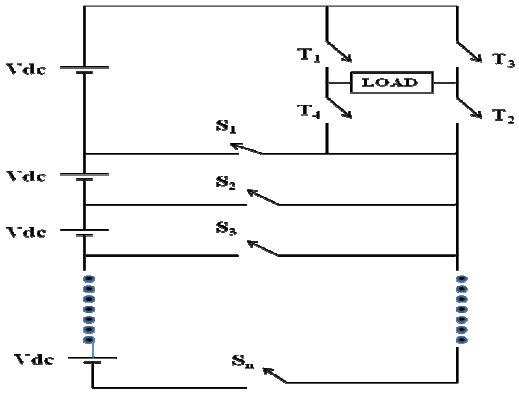


**Fig. 5:** Configuration of proposed Cascaded Multilevel Inverter.

Figure5 shows the circuit arrangement of proposed topology which consists of 'n' number of switches and the resistive load is used. Here the switches are IGBT. In both positive and negative voltages are reversed by switches such as $T_1, T_2, T_3 T_4$. Switches $T_1$&$T_2$ are used for positive polarity and the remaining switches $T_3$&$T_4$ are used for negative polarity. So the both positive and negative sides to produce the desired level waveforms.

*Operation For 9 Level:*

Figure6 shows the circuit arrangement of 9 level proposed topology which consists of eight switches and four DC sources are used. Switches $T_1$, $T_2$, $T_3$ and $T_4$ are used for reversal polarity and the remaining switches such as $S_1$, $S_2$, $S_3$ and $S_4$ are used to generate the levels in both positive and negative sides to produce the desired nine level waveforms. The switching sequence is displayed in Table 4.

The duration of different levels at the output changes each time, when the sine wave amplitude changes from one desired level to another, which makes the staircase output much more similar to a sine wave.

Table4. shows the switching sequence of the proposed 9 level topology. In this, the switching transition is minimum during each mode transfer so there is a reduction in the switching loss. Switches (S1-S4) are the level selection switches and switching pulses corresponding to each switches.

*Switching Summary:*

In this chapter discuss about switching comparison between an existing topology and proposed topology.

Switching requirements in the proposed multilevel inverter are simpler as compared to conventional topologies. There is no need to control negative cycle so it does not generate negative pulses. Thus, there is no need for extra conditions for controlling the negative voltage.

In Table.5. shows the switching requirement of the proposed topology. In this, the switching transition is minimum during each mode transfer so there is a reduction in the switching loss. Switches($S_1$-$S_n$) are the level selection switches and switching pulses corresponding to each switches.

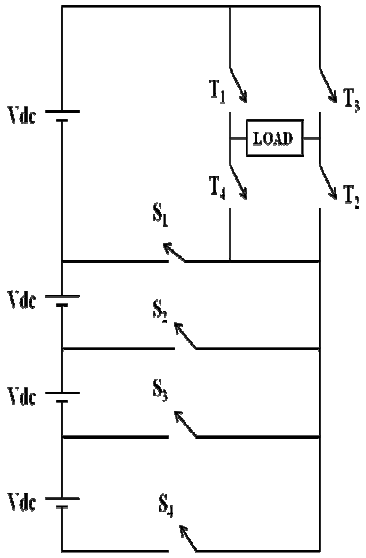


**Fig. 6:** Configuration of 9 level proposed Cascaded Multilevel Inverter.

**Table 4:** Switching sequence of 9 level proposed topology.

| $V_{out}$ | Switches State | | | | | |
|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $T_1$,$T_2$ | $T_3$,$T_4$ |
| $V_{dc}$ | on | off | off | off | on | off |
| $2V_{dc}$ | off | on | off | off | on | off |
| $3V_{dc}$ | off | off | on | off | on | off |
| $4V_{dc}$ | off | off | off | on | on | off |
| 0 | off | off | off | off | off | off |
| $-V_{dc}$ | on | off | off | off | off | on |
| $-2V_{dc}$ | off | on | off | off | off | on |
| $-3V_{dc}$ | off | off | on | off | off | on |
| $-4V_{dc}$ | off | off | off | on | off | on |

**Table 5:** Switching comparison.

| LEVEL | Number Of Switches | | | |
|---|---|---|---|---|
| | H-Bridge Multilevel Inverter | Existing Topology 1 | Existing Topology 2 | Proposed Topology |
| 5 | 8 | 8 | 7 | 6 |
| 7 | 12 | 10 | 9 | 7 |
| 9 | 16 | 12 | 11 | 8 |
| 11 | 20 | 14 | 13 | 9 |
| 13 | 24 | 16 | 15 | 10 |
| 15 | 28 | 18 | 17 | 11 |
| 17 | 32 | 20 | 19 | 12 |
| 19 | 36 | 22 | 21 | 13 |
| 21 | 40 | 24 | 23 | 14 |
| 23 | 44 | 26 | 25 | 15 |

*Simulation results:*

*Nine level :*

The simulation case study has been carried out software to validate the result. Figure 7. Shows the simulation model of 9 level the proposed topology.

To generate the 9 level output voltage, 8 IGBTs and four DC power source of 100 Volts are used. Pulses are generated by using nearest level control method. The simulated Output voltage is shown in Figure8. and the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

*Eleven level:*

The simulation case study has been carried out software to validate the result. Figure 10. Shows the simulation model of 9 level the proposed topology.

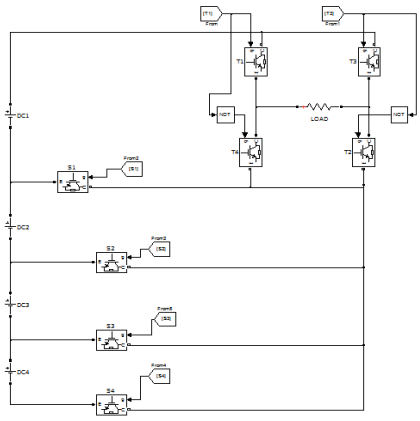

**Fig. 7:** Simulation diagram of 9 level proposed topology.

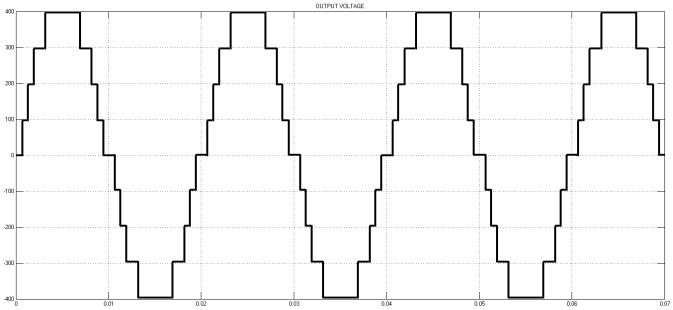

**Fig. 8:** Nine level output for proposed topology.

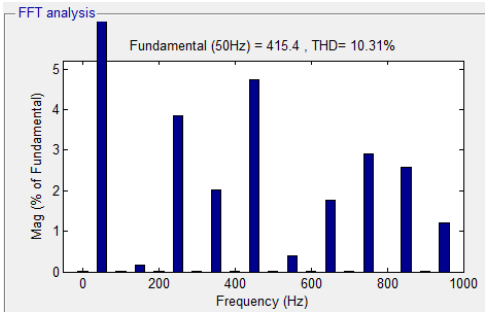


**Fig. 9:** Harmonics analysis of 9 level proposed topology.

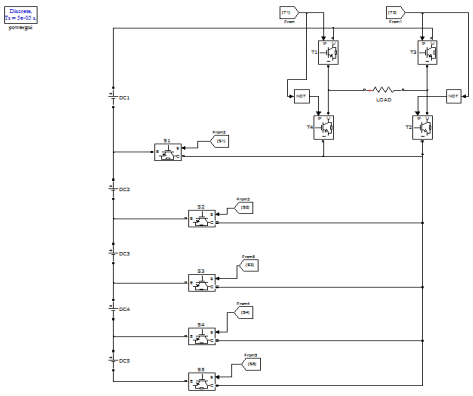

**Fig. 10:** Simulation diagram of 11 level proposed topology.

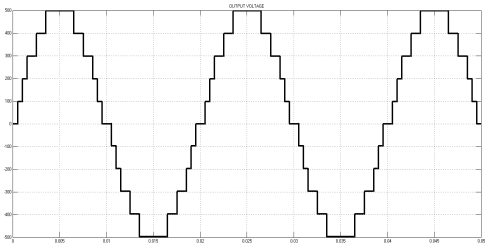

**Fig. 11:** Nine level output for proposed topology.

To generate the 11 level output voltage, 9 IGBTs and five DC power source of 100 Volts are used. Pulses are generated by using nearest level control method. The simulated Output voltage is shown in Figure8. and the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

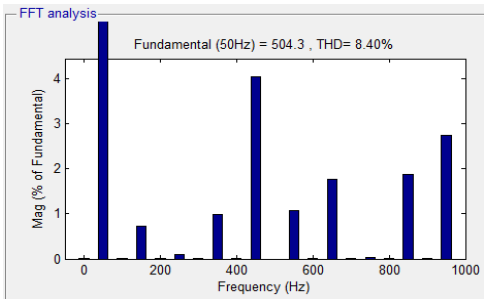


**Fig. 12:** Harmonics analysis of 9 level proposed topology.

*Fifteen Level:*

The simulation case study has been carried out software to validate the result. Figure13. Shows the simulation model of 9 level the proposed topology.

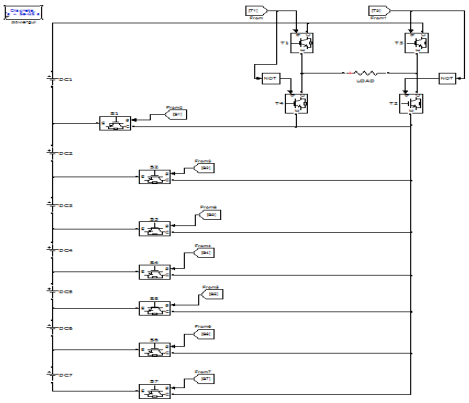

**Fig. 13:** Harmonics analysis of 15 level proposed topology.

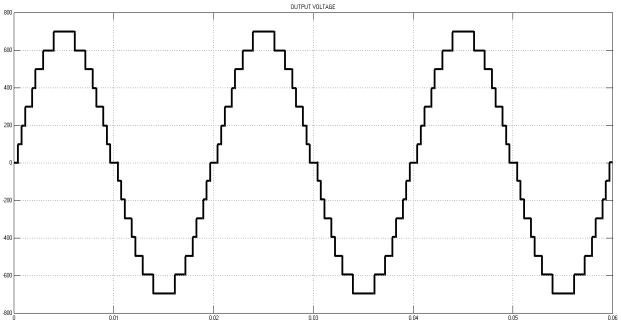

**Fig. 14:**

To generate the 15 level output voltage,11 IGBTs and four DC power source of 100 Volts are used. Pulses are generated by using nearest level control method. The simulated Output voltage is shown in Figure14. and the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

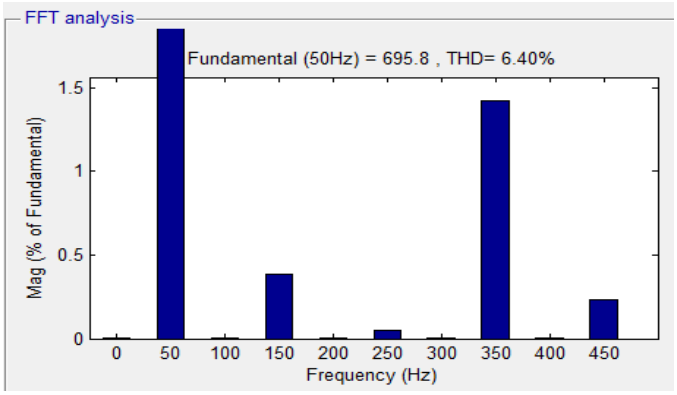


**Fig. 15:**

*Thd Summary:*

In Table 6. analysis the Total Harmonics Distortion (THD) of proposed topology.

**Table 6:**

| PROPOSED MULTILEVEL INVERTER | |
|---|---|
| LEVEL | THD |
| 5 | 20.94 % |
| 7 | 14.47 % |
| 9 | 10.31 % |
| 11 | 8.40 % |
| 13 | 7.70 % |
| 15 | 6.40 % |
| 17 | 5.86 % |

*Conclusion:*

A single phase new cascaded multilevel inverter topology has been shown to produce an increased stepped output with less number of semiconductor switches. With fewer switches, controlling the overall circuit becomes less complex, the size and installation area are reduced. Switching loss and THD are reduced as compared to conventional topologies. The proposed circuit is performing harmonic reduction with reduced no of switches. Simulation results using MATLAB is also provided to validate the design.

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