Novel Topology of Asymmetric Multilevel with Reduced Number of Switches Utilizing Photovoltaic Applications

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ABSTRACT

In this project, a new general diode clamped multilevel inverter using H-bridges. The proposed topology requires a lesser number of pv voltage sources and power switches. It consists of lower blocking voltage on switches in which the switching sequences are arranged in pulse width modulation, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies from aforementioned points of view. Moreover, a new algorithm is to determine the magnitude of dc voltage source is replaced by PV source is proposed. The performance and functional accuracy of the proposed topology using the new algorithm in generating all voltage levels for a 31-level inverter are confirmed by simulation and experimental results.

KEYWORDS: Asymmetrical multilevel inverter, Bidirectional switch, Total harmonic distortion (THD), Pulse width modulation inverters.

INTRODUCTION

Generally Multilevel inverters have received more attention for their ability on high-power and medium voltage operation and because of other advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference [1, 2]. These inverters generate a stepped voltage waveform by using a number of dc voltage sources as the input and an appropriate arrangement of the power-semiconductor-based devices [3]. Three main structures of the multilevel inverters have been presented: “diode clamped multilevel inverter,” “flying capacitor multilevel inverter,” and “cascaded multilevel inverter” [4]. The cascaded multilevel inverter is composed of a number of single-phase H-bridge inverters and is classified into symmetric and asymmetric groups based on the magnitude of dc voltage sources. In the symmetric types, the magnitudes of the dc voltage sources of all H-bridges are equal while in the asymmetric types.

A. Diode clamped multilevel inverter:

The diode clamped multilevel proposed by was named as neutral point converter and was essentially a five-level diode clamped inverter as shown in Fig. In this circuit, the dc-bus voltage by using two series-connected capacitors can split the supply voltage into three voltage levels and the midpoint of the capacitors is called the neutral point. The voltage output can have five output states: 2Vdc, Vdc, 0, -Vdc and -2Vdc. The diodes are being utilized for clamping the switch voltage to half the dc-bus voltage magnitude.
Fig. 1: Multilevel inverter topologies: five-level (a) DC-MLI, (b) FC-MLI, (c) CHB-MLI.

B. Flying Capacitor Inverter:

The fundamental building block of a five level flying capacitor inverter is shown in Fig. 2(b). Independent capacitors are used to clamp the device voltage for different voltage levels. The topology provides a five levels across the output: 2Vdc, Vdc, 0, -Vdc and -2Vdc. For voltage level 2Vdc, switches S1 and S2 need to be turned on; for -2Vdc, switches S1’ and S2’ is turned on. For the zero level, either pair (H1 and H4) or (H2 and H3) are turned on. Clamping capacitor C1is charged when H4 and H1 are turned on, and is discharged when H2 and H3are turned on. By having a proper selection of switch combination for different output levels, the charge of C1can be balanced. Even for this topology, the capacitor clamping, a large number of bulky capacitors are required to clamp the voltage as in case of diode clamping. If the voltage rating of each capacitor used is assumed to have the same voltage rating as that of the main power switch, an ‘m’ level converter requires about (m-1)(m-2)/2 numbers of per phase clamping capacitors and in addition to that the topology requires (m-1) numbers of main dc-bus capacitors

C. Cascaded Multilevel Inverters:

Similar to a two level single-phase inverter, a series connection of the same brings about a new converter topology with independent dc sources, which is shown in Fig. 2. Fig. 2shows the power circuit for a single phase leg of a five- level inverter with two H-bridges of four cells in each bridge. The resultant output voltage is synthesized by adding the voltages generated by the various cells. The circuitry generates five levels of voltages at the output: 2Vdc, Vdc, 0, -Vdc and -2Vdc. With different possible combinations of these switches, in the two H- bridges, the converter can generate five different voltage outputs in combination with the individual dc sources. The AC outputs of different full bridge converters in the same phase are connected accordingly so that the resultant output voltage waveform is the sum of all individual inverter outputs.

Even though various multilevel inverter structures are used, the Cascaded Multi-Level Inverter (CMLI) appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter [13]. A cascaded multilevel inverter eliminates the large number of large transformers requirements, clamping diodes requirements, as in a diode-clamped multilevel inverters and requirements of the flying capacitors, as required by flying- capacitor multilevel inverters. It also has the advantage of being more suitable to high-voltage, high-power applications, generates a multistep staircase voltage waveform approaching a pure sinusoidal output voltage by increasing the number of levels, it does not require voltage balance devices. As these features are considered highly advantageous, the cascaded multilevel inverter topology is preferred as an important alternative in the medium-voltage level inverter configurations.

Modulation Technique:

Mainly power electronic converters are operated in the “switched mode” which means the switches within the converter are always in either one of the two states - turned off (no current flows), or turned on (saturated with only a small voltage drop across the switch). Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, leads to high switching power losses resulting in reduction of efficiency. As a measure to control this power flow, the switches are made to alternate between these two states (i.e. on and off). The switched component is eliminated and retention of the desired components of dc or low frequency ac is done which is called Pulse Width Modulation (PWM), as the pulse width is modulated to control the desired average output value. Several modulation and control strategies have been developed or adopted for multilevel inverters including the following: Multilevel sinusoidal pulse width modulation (SPWM), multilevel selective harmonic elimination (SHE), and space-vector modulation (SVM). In a conventional two-level inverter configuration, the harmonic reduction of an inverter output current is achieved mainly by raising the switching frequency. But in high power applications, the switching frequency of the
power device has to be restricted below 1 KHz due to the increased switching losses and also the level of dc-bus voltage.

Based on the switching frequency, modulation methods used in multilevel inverters can be classified as shown in Fig. 3. Modulation techniques are mainly classified based on the number of commutations made per cycle. Modulations made with either one or two commutations of the power semiconductors per cycle of the output voltages, generating a staircase waveform are classified under low switching frequency modulation and those converters that performs multiple commutations per cycle of the output voltages fall under high switching frequency modulation.

Multilevel Selective Harmonic Elimination(SHE) and the space-vector control (SVC) are classified under low switching frequency modulation technique. Space-Vector PWM (SVPWM) and Carrier-based Sinusoidal PWM (SPWM) mainly fall under High Switching Frequency PWM.

Many new modulations have been developed to cater to the growing number of MLI topologies. They are aimed at generating a stepped switched waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency and phase fundamental component that is usually a sinusoid in steady state. It is necessary that the modulation scheme is intended to be used in high-power converters, the intended outcomes necessitates power quality and minimum switching losses. These are contradictory with each other, and therefore, it is considered one of the major challenges in MLI technology [13].

SVPWM(Space-vector PWM) strategy can be utilised as another alternative, which is an efficient modulation technique. It generally have the following features: efficient utility of the dc-link source voltage, less current ripple, and easier implementation by a DSP processor which are considered favorable features for high-voltage high-power applications. As the number of levels increases, redundant switching states and the complexity of selecting switching states increases.

Selective harmonic elimination PWM (SHE-PWM) technique is a modulation based on fundamental frequency switching theory proposed in 1974, which aims at eliminating defined harmonic content orders. The main idea of this method is based on defining the switching angles of harmonic orders to be eliminated to minimize voltage THD ratio and obtaining the Fourier series expansion of output voltage. Since the parameters obtained by the Fourier series expansion are nonlinear, the values have to be obtained using Newton-Raphson Iterations where possible switching angles are calculated previously and saved in a look-up tables in an independent memory. The main defect of SHE-PWM is the requirement of calculations to determine switching angles as in fundamental frequency switching method. However, Newton-Raphson Iteration is able to solve the Fourier series while the initial values are based on assumptions and the with imprecise results.

The carrier-based Sinusoidal PWM schemes used for multilevel inverters can be classified into phase-shifted modulation and level-shifted modulation both of which can be applied to the cascaded H-bridge (CHB) inverters. As the THD of phase-shifted modulation is much higher than level-shifted modulation, for achieving lesser THD, level-shifted modulation is generally used. A ‘m’ level CHB inverter using level-shifted multicarrier modulation scheme needs (m-1) numbers of triangular carriers signals, with the same amplitude and frequency. The (m-1) numbers of triangular carriers are vertically arranged in such a way that the bands they occupy are contiguous. There are four methods of phase disposition of carrier bands as classified by Carrara [7], [8]. Based on the phase relationships of different levels, there can be PWM strategies as follows: i) In-phase disposition (IPD), where all the carriers signals in the multilevel space are in phase with each other in the different levels ii) Phase opposition disposition (POD), where the carrier bands are in phase above the zero reference and with a phase shift of 180 degree below the zero iii) Alternative phase opposition disposition (APOD) where there is a phase shift by 180 degree between each carrier band with that of the alternate carrier waveform or iv) Phase Disposition (PD), in which all the carrier waves are shifted by a phase angle of 2/(N-1) radians. The multilevel pulse width modulation (PWM) converter topology is recently being utilised in the power industry since it caters to the requirement of high power applications like Static Var Compensation,
active power filters, and high power adjustable frequency drives [9, 10]. As both amplitude and pulse width modulations can be efficiently done in these multilevel topologies, the quality of the output waveform thus obtained will be high with low harmonic distortion [11].

Two topologies are existed for a seven-level inverter. Then the topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed topologies are comprised of six unidirectional power switches ($S_1, S_2, S_3, S_4, S_5,$ and $S_6$) and two dc voltage sources ($V_{L1}$ and $V_{R1}$). In this paper, these topologies are called developed H-bridge. The simultaneous turn-on of SL1 and SL2 (or SR1 and SR2).Numerous industrial applications have begun to require higher power apparatus in recent years. Power-electronic inverters are becoming popular for various industrial drives applications [2]. A multilevel inverter is a power electronic system that synthesizes a desired output voltage.

In recent years, several topologies with various control techniques have been presented for cascaded multilevel inverters [5-8]. In [4, 9-15], different symmetric cascaded multilevel inverters have been presented. The main advantage of all these structures is the low variety sources, which is one of the most important features in determining the cost of the inverter. On the other hand, because some of them use a high number of bidirectional power switches, a high number of insulated gate bipolar transistors (IGBTs) are required, which is the main disadvantage of these topologies. An asymmetric topology has been presented in [6]. The main disadvantage of this structure is related to its bidirectional power switches, which cause an increase in the number of IGBTs and the total cost of the inverter. In [5], a new topology with three algorithms have been presented, which reduce the number of required power switches but increase the variety of dc voltage sources. In [1, 4, 7, 8], several algorithms for determining the magnitudes of dc voltage sources for the conventional cascaded multilevel inverter have been presented.

The major advantage of this topology and its algorithms is related to its ability to generate a considerable number of output voltage levels by using a low number of sources and power switches but the high variety in the magnitude of dc voltage sources is their most remarkable disadvantage. In this paper, in order to increase the number of output voltage levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of diode clamped multilevel inverters is proposed.

It is important to note that in the proposed topology, the unidirectional power switches are used. Then, to determine the magnitude of the dc voltage sources, a new algorithm is proposed. Moreover, the proposed topology is compared with other topologies from different points of view such as the number of IGBTs, number of pv sources, the variety of the values of the pv voltage sources, and the value of the blocking voltages per switch. Finally, the performance of the proposed topology in generating all voltage levels through a 31-level inverter is confirmed by simulation using (MATLAB) software results

**Circuit diagram and operation:**

Diode clamped inverter is the one of the important topologies in the family of multilevel inverter. The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. It is more efficient for back to back high power connections and high efficiency for switching fundamental frequency(50Hz). A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage.. This problem can be solved by increasing the switches, diodes, capacitors. Due to the capacitor balancing issues, these are limited to the three levels.

This type of inverters provides the high efficiency because the fundamental frequency used for all the switching devices and it is a simple method of the back to back power transfer systems. The new topologies of clamped multi level inverter with h bridge are proposed for 31-level inverter as shown in fig 1. The proposed topology are comprised by adding four bidirectional switches and one H-bridge inverter structure ($S_1, S_2, S_3, S_4, H_1, H_2, H_3, H_4$) and four voltage sources($Vs1, Vs2, Vs3, Vs4$). The simultaneous turn –on of the switches causes the voltage sources into short circuit.

So the simultaneous turned on of the mentioned switches switches should be avoided.1 and 0 indicates ON and OFF states of the switches respectively. The generalized single-phase structure of the proposed topology has n number of isolated input sources. The link age structure is such that the higher potential terminal of the preceding source is connected to the lower potential terminal of the succeeding source and vice versa through power switches.

The switching pulses shows that switches $H1$ and $H3$ operate at a fundamental frequency of 50 Hz while switches $T1, T1, T3$, and $T4$ operate at a frequency of 1 kHz. Thus, low-voltage-rated switches operate at high frequency and incur more switching losses, while high-voltage rated switches operate at fundamental frequency and incur more conduction losses. In this manner, the total losses among the switches get distributed. The waveforms for RL load voltage and its harmonic spectrum.

The values of pv voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources. considering the aforementioned explanations, the total cost of the proposed topology in Fig. 1 is low because voltage sources with low magnitudes are needed.
In the proposed general topology, the number of output voltage levels ($N_{\text{step}}$), number of switches ($N_{\text{switch}}$), number of dc voltage sources ($N_{\text{source}}$), and the maximum magnitude of the generated voltage ($V_{\text{max}}$) are calculated as follows, respectively:

$$N_{\text{switch}} = 4N + 2$$  \hspace{1cm} (1)
$$N_{\text{source}} = 2N$$  \hspace{1cm} (2)

The above equations are number of switches, number of sources and maximum average output voltage respectively.

Where, $N_{\text{step}}$ — number of output level

Here PV panel is used for a complex piece of equipment made up of thousands of components. Roughly 80% of losses come from a switching device. One of the most critical components within PV inverter is this “switching device” or semiconductor device being used to perform DC to AC conversion. The solar industry has relied on an IGBT (Insulated Gate Bi-polar Transistor) for this device. The IGBT is the heart of the PV inverter where power conversion really takes place.

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values of dc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter’s total cost decreases.
Fig. 5: Triggering of switching pulses.

Output voltage can be determined by below equations.

The number of variety of the values of dc voltage sources is given by

\[ N_{\text{variety}} = 2^n \]  \hspace{1cm} (3)

The magnitudes of the dc voltage sources of the proposed 31-level inverter are recommended as follows:

\[ V_{S1} = V_{DC} \] \hspace{1cm} (4)
\[ V_{S2} = 2V_{DC} \] \hspace{1cm} (5)
\[ V_{S3} = 5V_{DC} \] \hspace{1cm} (6)
\[ V_{S4} = 10V_{DC} \] \hspace{1cm} (7)

The proposed inverter can generate all negative and positive voltage levels from 0 to 15V dc with steps of \( V_{dc} \).

\[ N = 2n + 1 \] \hspace{1cm} (8)

The peak voltage attained for such a configuration is given by

\[ V_{\text{max}} = nV_{dc} \] \hspace{1cm} (9)

Experimental results and discussions:

Fig. 6: Output voltage and current waveform for 31 level inverter.

The output voltage and current waveform of 31 level inverter shown in fig 3. The supply voltages are 22V, 43V, 86V and 173V respectively.
The simulated output voltage and current waveforms are shown in Fig. 2. The proposed topology is able to generate 31 levels (15 positive levels, 15 negative levels, and 1 zero level) with the maximum voltage of 225 V. Comparing the output voltage and current waveforms indicates that the output current waveform is more similar to the ideal sinusoidal waveform than the output voltage because the $R-L$ load acts as a low-pass filter. In addition, there is a phase difference between the output voltage and current waveforms, which is caused by the inductive feature of the load. The total harmonic distortions of the output voltage and current are equal to 4.51% respectively.

The harmonic spectrum of the output voltage and current respectively. The figure shows that the magnitudes of harmonics of both voltage and current waveforms are low. However, the harmonics of the current waveform are lower than the voltage waveform.

High-switching-frequency modulation methods like multi-carrier PWM and space vector modulation techniques have been used for MLI modulation control. On the other hand, active harmonic elimination, selective harmonic elimination, and fundamental frequency method are considered as low-switching-frequency methods. The proposed topology can be modulated with anyone of these methods with suitable adaptation. In the present work, the multicarrier PWM scheme is used.

### Table 1: Switching sequence of positive half cycle

<table>
<thead>
<tr>
<th>LEVELS</th>
<th>T1</th>
<th>T2</th>
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<th>H1</th>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>14</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>15</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>16</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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</tbody>
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The simulations done by MATLAB software. According to the maximum output voltage of the inverter will be 225V.

In a multicarrier PWM scheme, carrier signals are compared with the reference signal and the pulses obtained are used for switching of devices corresponding to respective voltage levels. In the proposed topology, one switch may contribute for synthesis of more than one level at output terminals. Moreover, proper utilization of six modes (viz., modes 1, 2, 3, 5, 6, and 8) will lead to fundamental switching of T2 and T2 which bear voltage stress of 2Vdc each as compared to the remaining switches which bear voltage stress of Vdc each.

**Conclusion:**

The basic topologies can be developed to any number of levels at the output where the 31-level and general topologies are consequently presented. In addition, a new algorithm to determine the magnitude of the PV voltage sources has been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison results, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and switches. However, the proposed topology has a higher number of variety of PV sources in comparison with the others. The performance accuracy of the proposed topology was verified through the MATLAB simulation results of a 31-level inverter.

**REFERENCES**