Performance Analysis of A Low Power High Speed Hybrid 1-Bit Full Adder Circuit

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Received 25 January 2016; Accepted 18 April 2016; Available 28 April 2016

ABSTRACT

Full adder is one of the most fundamental building block of all the circuit applications. Most full adder systems are considered performance of speed, chip area, threshold loss, full swing output, delay and the most important is power consumption. The increasing demand for the high fidelity devices has laid emphasis on the development of high speed, low power and high performance systems. So the 1-bit full-adder circuit is very important component in the design of application specific integrated circuits. This paper presents a low power high speed hybrid 1-bit full adder circuit. Full adder designs use more than one logic style which is known as hybrid logic design style. The hybrid 1-bit full adder circuit is a important building block of the application of VLSI. Hybrid 1-bit full adder circuit is based on different logic styles because the different logic style is used to improve the overall performance of the full adder. Proposed hybrid 1-bit full adder circuit is designed for modified XNOR module and carry generation module by using PMOS and NMOS transistors. The modified XNOR module generates the sum signal and it is used to improve the speed of full adder circuit. Carry generation module generates the carry signal and it is used to reduce the propagation delay of full adder circuit. The hybrid 1-bit full adder circuit design can be realized in 180-nm technology and analyse the performance of propagation delay, power, speed and total nodes.

KEYWORDS:

INTRODUCTION

Today demand and popularity of the battery- operated portable devices such as cellular phone, laptop computers, tablet and personal digital assistant (PDA) is increasing that depends on high speed, small size, high reliability, low power consumption and longer battery life that demand for VLSI. Full adders, being one of the most fundamental building blocks of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years [1]. Different logic styles, each having its own merits and bottlenecks, was investigated to implement 1-bit full adder cells [2]. The designs, reported so far, may be broadly classified into two categories: 1) static style and 2) dynamic style. Static full adders are generally more reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart [3]. Different logic styles tend to favor one performance aspect at the expense of others. Standard static complementary metal oxide semiconductor (CMOS), dynamic CMOS logic, complementary pass transistor logic (CPL) [4] and transmission gate full adder (TGA) [5], [6] are the most important logic design styles in the conventional domain. These designs exploit the features of different logic styles to improve the overall performance of the full adder. The advantages of standard complementary (CMOS) style based adders transistors are its robustness against voltage scaling and transistor sizing, while the disadvantages are high input capacitance and requirement of buffers. Another complementary type smart design is the mirror adder with almost same power consumption and transistor count (as that of but the maximum carry propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder [7]. On the other hand, CPL shows good voltage swing restoration employing 32 transistors. However, CPL is not an appropriate choice for
low-power applications [8]. Because of its high switching activity of intermediate nodes (increased switching power), high transistor count, static inverters and overloading of its inputs are the bottlenecks [9] of this approach. The prime disadvantage of CPL, that is, the voltage degradation was successfully addressed in TGA, which uses only 20 transistors for full adder implementation. However, the other drawbacks of CPL like slow-speed and high-power consumption remain an area of concern for the researchers [10]. Later, researchers focused on the hybrid logic approach which exploited the features of different logic styles in order to improve the overall performance.

2. Design Approach Of The Proposed Full Adder:

The proposed full adder circuit is represented by three blocks such as module 1 and module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the carry signal (C_{out}). The schematic structure of the proposed full adder circuit is shown in figure 1.

![Schematic structure of hybrid 1-bit full adder](image)

**Fig. 1:** Schematic structure of hybrid 1-bit full adder

Where,

- A, B, C_{in} - Three inputs
- SUM, C_{out} - Output

Each module is designed individually such that the entire adder circuit is optimized in terms of power, delay, and area. The modified XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility.

2.1 Modified XNOR Module Circuit:

The modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors being small) formed by transistors Mp1 and Mn1. The modified XNOR module circuit is shown in figure 2.
Fig. 2: Modified XNOR module circuit

Where,
Mp - PMOS transistor, PMOS - P-channel metal oxide semiconductor
Mn - NMOS transistor, NMOS - N-channel metal oxide semiconductor

Full swing of the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3. The XNOR module employed six transistors (6T) (three PMOS transistors and three NMOS transistors). Because the six transistors (6T) are used to minimize the power consumption of the overall full adder circuit.

2.2 Carry Generation Module Circuit:
The output carry signal is implemented by the transistors Mp7, Mp8, Mn7, and Mn8. The input carry signal \( (C_{in}) \) propagates only through a single transmission gate (Mn7 and Mp7), reducing the overall carry propagation path significantly. The carry generation module circuit is shown in figure 3.

Fig. 3: Carry generation module circuit

The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8, and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal. Modified XNOR module and carry generation module circuit is designed individually by using p-channel metal oxide semiconductor (PMOS) and n-channel metal oxide semiconductor (NMOS) transistors.

3. Detail Circuit Diagram Of Proposed Full Adder:
The hybrid 1-bit full adder circuit has 16 transistors such as eight PMOS transistors and eight NMOS transistors. The sum output of the full adder is implemented by XNOR modules. The inverter comprised of
transistors $M_{p1}$ and $M_{n1}$ generate $B'$, which is effectively used to design the controlled inverter using the transistor pair $M_{p2}$ and $M_{n2}$. Proposed full adder circuit is shown in figure 4.

Fig. 4: Hybrid 1-bit full adder circuit

The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors $M_{p1}$ and $M_{n1}$ generate $B$, which is effectively used to design the controlled inverter using the transistor pair $M_{p2}$ and $M_{n2}$. Output of this controlled inverter is basically the XNOR of $A$ and $B$. But it has some voltage degradation problem, which has been removed using two pass transistors $M_{p3}$ and $M_{n3}$.

The PMOS transistors ($M_{p4}$, $M_{p5}$, and $M_{p6}$) and NMOS transistors ($M_{n4}$, $M_{n5}$, and $M_{n6}$) realize the second stage XNOR module to implement the complete SUM function. If they are same, then $C_{out}$ is same as $B$, which is implemented using the transmission gate realized by transistors $M_{p8}$ and $M_{n8}$. Otherwise, the input carry signal ($C_{in}$) propagates only through a single transmission gate ($M_{n7}$ and $M_{p7}$). If they are same, then $C_{out}$ is same as $B$, which is implemented using the transmission gate realized by transistors $M_{p8}$ and $M_{n8}$. Otherwise, the input carry signal ($C_{in}$) is reflected as $C_{out}$ which is implemented by another transmission gate consisting of transistors $M_{p7}$ and $M_{n7}$. It is likely that a single bit adder cell designed for optimum performance may not perform well under deployment to real time conditions.

3.1 180-nm technology:

The 180-nm technology is a transistor length of the hybrid 1-bit full adder circuit.

<table>
<thead>
<tr>
<th>Transistor name</th>
<th>180-nm technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Width ($W$) (nm)</td>
</tr>
<tr>
<td>$M_{n1}$, $M_{n6}$</td>
<td>400</td>
</tr>
<tr>
<td>$M_{p1}$, $M_{p6}$</td>
<td>800</td>
</tr>
<tr>
<td>$M_{n2}$, $M_{n3}$</td>
<td>400</td>
</tr>
<tr>
<td>$M_{p2}$, $M_{p3}$</td>
<td>800</td>
</tr>
<tr>
<td>$M_{n4}$, $M_{n5}$</td>
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<td>$M_{p4}$, $M_{p5}$</td>
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<tr>
<td>$M_{n7}$, $M_{n8}$</td>
<td>400</td>
</tr>
<tr>
<td>$M_{p7}$, $M_{p8}$</td>
<td>400</td>
</tr>
</tbody>
</table>

3.2 Performance analysis:

1. Power:

The performance of the proposed full adder in terms of propagation delay, speed, transistors count, total nodes, total devices and temperature level. Power consumption of the hybrid full adder can be broadly classified into two categories

- Static power and
- Dynamic and short-circuit power
Static power, originated from biasing and leakage currents, in most of the CMOS-based implementations is fairly low when compared with its dynamic counterpart. The transistor size could be an effective parameter for reducing dynamic power consumption.

2. Delay:
In the present design, the carry signal is generated by controlled transmission of the input carry signal and either of the input signals A or B (when \( A = B \)). As the carry signal propagates only through the single transmission gate, the carry propagation path is minimized leading to a substantial reduction in propagation delay.

The delay incurred in the propagation is further reduced by efficient transistor sizing and deliberate incorporation of strong transmission gates. However, during cascaded operation of the proposed full adder, operating in the carry propagation mode, the speed performance of the adder deteriorates with increase in the number of adder stages.

3. Speed:
Full adder is the fundamental computational unit in most of the systems, its delay predominantly governs the overall speed performance (Vivek kumar et.al 2012) of the entire system. Also, the speed of response of an adder is mainly dependent on the propagation delay of the carry signal which is usually minimized by reducing path length of the carry signal.

4. Transistors Count:
The transistors count of the proposed full adder is given by using 16 transistors for 8- PMOS transistors and 8- NMOS transistors. It is used to minimize the chip size and minimize the noise of the overall full adder circuit.

6. Total Devices:
The total devices are used to reduce the power dissipation of the overall full adder circuit. It is consists of two types
- Active devices
- Passive devices
An active devices or components which are required external source to their operation are called active devices. It is used to produce energy in the form of voltage or current. Active devices are transistors and vacuum tubes.

3.3 Existing system:
Proposed full adder design and performance is compared with the existing system of the conventional CMOS full adder designs

3.3.1 Conventional CMOS full adder:
The conventional CMOS full adder circuit is shown in figure 7.

[Diagram of Conventional CMOS full adder circuit]

Fig. 5: Conventional CMOS full adder circuit
The conventional CMOS full adder cell has 28 transistors. Different logic styles can be investigated from different points of view. Evidently, they tend to favor one performance aspect at the expense of others. In other words, it is different design constraints imposed by the application that each logic style has its place in the cell library development. Even a selected style appropriate for a specific function may not be suitable for another one.

4 Simulation Results:
4.1 Hybrid 1-bit full adder design:

Hybrid 1-bit full adder is designed for modified XNOR module and carry generation module. Modified XNOR module is used to generate the sum signal and minimize the power, improve the speed of the hybrid 1-bit full adder.

The hybrid 1-bit full adder circuit has 16 transistors and it is implemented by using Tanner EDA tool is shown below figure 6 &7.

![Fig. 6: Hybrid 1-bit full adder design](image)

![Fig. 7: Output of hybrid 1-bit full adder](image)

Hybrid 1-bit full adder is designed for modified XNOR module and carry generation module. Modified XNOR module is used to generate the sum signal and minimize the power, improve the speed of the hybrid 1-bit full adder. Carry generation module is used to generate the carry signal and reduce overall propagation delay of the hybrid 1-bit full adder. The 180nm technology is a transistor length of the hybrid 1-bit full adder. This technology is used to reduce the chip size of the full adder.

4.2 Conventional CMOS full adder design:

The conventional CMOS full adder circuit is implemented by using Tanner EDA tool. Conventional CMOS full adder circuit design is shown below in figure 8 & 9.
Fig. 8: Conventional CMOS full adder design

For example, static approach presents robustness against noise effects, so automatically provides a reliable operation. The issue of ease of design is not always attained easily. The CMOS design style is not area efficient for complex gates with large fan-ins. Thus, care must be taken when a static logic style is selected to realize a logic function. The conventional CMOS full adder cell has 28 transistors. Different logic styles can be investigated from different points of view. Evidently, they tend to favor one performance aspect at the expense of others.

4.3 Comparison performance analysis of existing and proposed system:
The comparison chart of hybrid 1-bit full adder and conventional CMOS full adder is shown in figure 10.
Conclusion:
A new low power high speed hybrid 1-bit full adder circuit design is proposed in this project. Hybrid 1-bit full adder circuit was designed by using 16 transistors with 180-nm technology. The 180-nm technology is a transistor length of the hybrid 1-bit full adder circuit. The performance of the hybrid 1-bit full adder circuit consumes low power (1.45 mw), low propagation delay (1.66 ps), high speed (1.48 seconds) and total devices (20) compared with the conventional CMOS full adder circuit consumes high power (2.93 mw), high propagation delay(1.70 ps), low speed (2.12 seconds) and total devices (32).

REFERENCES

