

Design of Low Power Bulk Driven Current Generator Based Subthreshold Cmos Circuit

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ABSTRACT

The paper deals with design of voltage reference circuit. The main part of the voltage reference circuit is to design of bulk driven and current trimming based sub threshold voltage reference circuit. This circuit is used to reduce the operation voltage level and overall power consumption level. Then the enhancement work is compensated sub-threshold CMOS design based on voltage reference circuit. This design is to reduce the transistor count level. This enhancement circuit consists of active load, voltage reference and starts up circuit level. A voltage reference circuit operating with all transistors biased in weak inversion, providing a mean reference voltage of 250 mV. This enhancement design is to reduce the overall power consumption level and to maintain the threshold voltage in any input voltage level.

KEYWORDS:

INTRODUCTION

In many applications, a precise and stable reference voltage is widely used in digital and analog circuits like analog–digital (A/D) and digital–analog (D/A) converters, voltage regulators, DRAM/flash memories and other communication devices. The demands for smaller area, low power consumption and low sensitivity to the supply voltage and temperature are getting increased. Recently, the voltage reference circuits were proposed to achieve smaller area without resistors, or low power supply, such as 1 V. However, all of them require big-area diodes or parasitic bipolar junction transistors (BJTs) with turn-on voltage as high as 0.6 V at room temperature. Thus, some people started to exploit MOSFETs operated in sub-threshold region to generate the reference voltage independent of the power supply and temperature, while reduce the chip area and power dissipation. However, the former one is focused on constant reference current. It requires a thermal-independent grounded resistor to convert to the desired reference voltage. The latter can generate a good reference voltage, but is more complicated than the one proposed in this brief. The battery-operated CMOS based electronic devices market is growing every year. To increase battery life, it is required to design circuit building blocks with lower supply voltage and consuming sub-microwatt power. Among them voltage reference circuits are essential in any CMOS design. They are used in almost all analog and digital systems to generate a DC voltage independent of the supply voltage and of temperature variation. Some of the systems on chip (SOC's) have special modes called sleep or standby modes, in which only a small part of the SOC is functional and the main part is switched off. It is quite possible that the SOC may spend long durations in these modes. To save the battery life, the SOC's should consume as low power as possible. They are normally required to consume power is sub-microwatts. Reference circuits are usually required to operate under these modes. Our target is to meet the power consumption for the reference circuits in nano-watts.

Band gap reference circuit is widely used to provide stable current and voltage references in analog circuits as well as in mixed signal CMOS circuits. A stable reference circuit should be robust against temperature, power supply and process variations. Sub 1V reference generation has got importance due to scaling resulting in shrinkage of MOS dimensions and reduction of power supply to minimize power consumption. Resistors occupy large area on the chip and hence increase the cost. On chip tolerance of resistors vary from 20% to 30%. So we have replaced these components with MOS transistors to improve performance of BGR and to save chip area. The combination of different operating regions like sub threshold, linear and saturation of MOS suppresses the temperature dependence of voltage reference.

The band gap voltage reference (BGR) circuit is an important component of Analog-to-Digital and Digital-to-Analog converters, which are broadly used in mixed-signal and radio-frequency systems. Most BGR use bipolar junction transistors (BJT) to easily reduce the temperature dependence, due to temperature coefficients, other common practice is the use of operational amplifiers (OP-AMP). With the reduction of the transistors size, and the reduction of supply voltage, more precise BGR circuits are needed. With 5 V supply, a band gap output voltage of 2 V with 20 mV variation is 1% error. With 2 V supply voltage, output of 1 V and the same 20 mV variation, the error is 2% error. The aim of this work is to realize an all CMOS Band gap. The study of new band gap circuit with CMOS technology, without BJT, is done throughout this paper. Another feature is the reduction of the circuit area since Operational-Amplifiers are not used.

II. Related Work:

Voltage reference generator circuits find application in multiple quarters such as flash memories, analog to digital and digital to analog converters and analog signal processing systems. Due to extensive use of reference voltage generators, there is a need for a reference-voltage generator circuit which is independent of variations in supply voltage, process parameter as well as temperature [1]. The temperature stability is improved by second-order compensation [2]. By employing a bulk-driven technique and the MOS transistors working in the sub threshold region, the supply voltage and the power dissipation are reduced.

III. Construction Of Bulk Driven Circuit Architecture:

Measurements performed over a set of 40 samples showed an average temperature coefficient of 165 ppm/°C with a standard deviation of 100 ppm/°C, in a temperature range from 0 to 125°C. The mean line sensitivity is $\approx 0.44\%/V$, for supply voltages ranging from 0.45 to 1.8 V. The power supply rejection ratio measured at 30 Hz and simulated at 10 MHz is lower than -40 dB and -12 dB, respectively. The active area of the circuit is $\approx 0.043\text{mm}^2$. This paper presents a CMOS voltage reference design, which is widely used in electronic circuits, both analog and digital circuits. In the conventional, a CMOS voltage reference circuit design composed of several MOS transistors and complicated circuits, the output voltage cannot be adjusted to any levels.

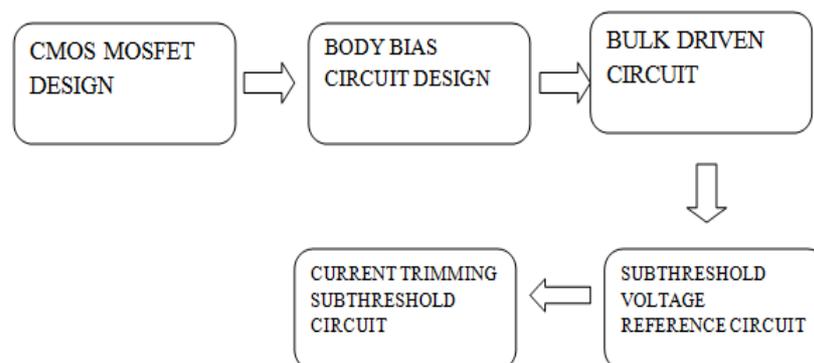


Fig. 1: Block diagram of Proposed Bulk Driven Architecture

A voltage reference circuit operating with all transistors biased in weak inversion, providing a mean reference voltage of 257.5 mV has been fabricated in 0.18 μm CMOS technology. The reference voltage can be approximated by the difference of transistor threshold voltages at room temperature. Accurate sub threshold design allows the circuit to work at room temperature with supply voltages down to 0.45 V and an average current consumption of 5.8 nA. Measurements performed over a set of 40 samples showed an average temperature coefficient of 165 ppm/°C with a standard deviation of 100 ppm/°C, in a temperature range from 0 to 125°C. The mean line sensitivity is $\approx 0.44\%/V$, for supply voltages ranging from 0.45 to 1.8 V.

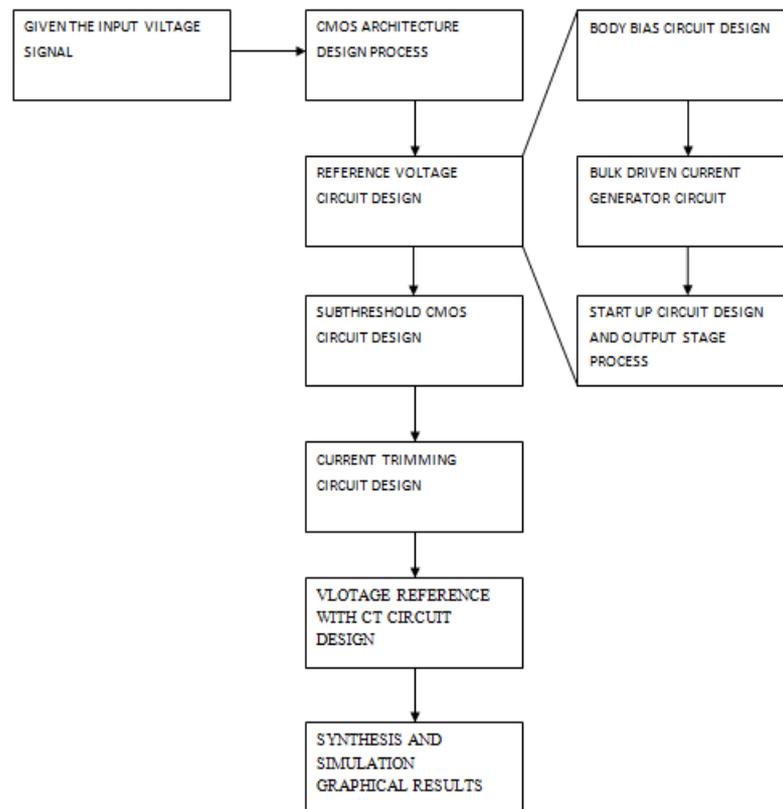


Fig. 2: Flow Chart of Proposed Bulk Driven Architecture

Bulk driven circuit is used to operate linear region and current trimming is used to compensate bias input voltage. Proposed system is to implement MOSFET based sub-threshold reference voltage circuit and to work is low input voltage level. To convert a signal, digital to analog or analog to digital, a reference voltage is needed. Furthermore being considered an auxiliary circuit, their function makes band gap voltage reference one of the most important circuits in all mixed-signal and radio-frequency systems. It is not possible to make a precise conversion if the voltage reference is not constant. Generic mixed-signal systems have more than one voltage reference as a result different voltage references are necessary.

A .Bulk Driven Current Generator Technique:

Proposed Bulk driven current generator circuit is used to set the threshold voltage in linear region level. This design is to maintain the input voltage VDD leakage level. This technique is to set nano ampere regime current reference. This design is to satisfy the resistor less voltage reference process work. This design is to optimize the analog devise and mostly using a MOSFET transistor based sub threshold voltage reference circuit designs.

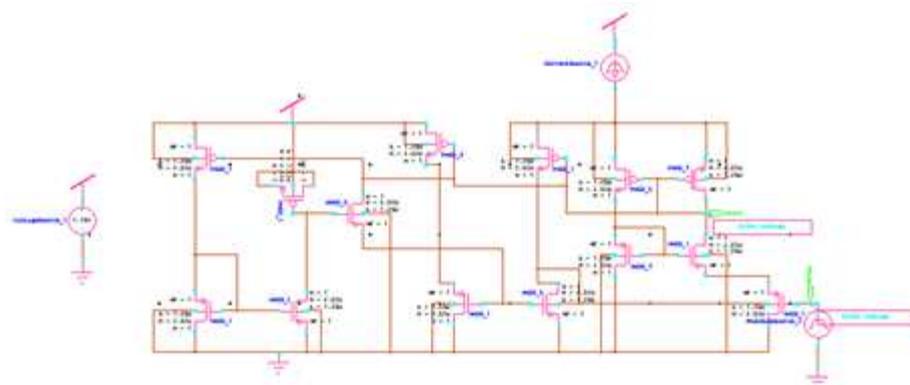


Fig. 3: schematic diagram for proposed Bulk Driven circuit

The core of the proposed sub threshold CMOS reference circuit is illustrated in Fig. 2. The circuit consists of a startup circuit, a bulk-driven current generator, a body-bias circuit, and an output stage. All the MOSFETs, except for M5 and M6, are operated in the sub threshold region. MOS resistor M5 is operated in a strong-inversion deep-triode region, and M6 is in the saturation region. The body-bias circuit provides a body bias voltage (V_{GS} , M14, i.e., the gate-source voltage of M14) to achieve temperature compensation. The positive TC voltage ΔV_{GS} (the gate-source voltage difference between M12 and M11 when the substrate of M11 is connected to ground) and the negative TC voltage V_{GS} , M14 are combined together to generate a temperature-independent V_{REF} .

B. Current Trimming Sub threshold Design:

Current trimming sub threshold circuit is used to set the stable threshold output voltage level. This design is to implement the current trimming function for dynamically set the output voltage. Current trimming circuit variation based on positive and negative direction and to set dynamic voltage variation. This design is to identify the deviation of voltage reference level and to reduce the overall threshold device power consumption and input voltage.

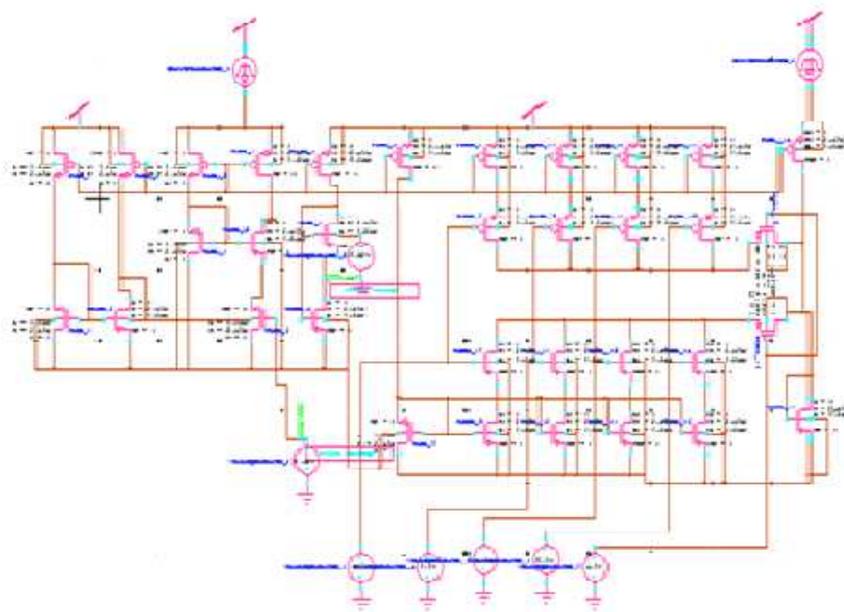


Fig. 3: schematic diagram for Current Trimming Circuit

The performance of the proposed circuit is confirmed through PSPICE simulation results, the circuit can be operated with supply voltage varies from 1.85 - 4V, and low power dissipation is 5.51 μW . Therefore, in this paper presents the CMOS voltage reference circuit design based on the new current summation technique that have opposite temperature coefficient for reference voltage generation which stabilized over process, supply voltage and temperature variations and proposed circuit is able to operate without complex startup circuit which this technique was reduced number of MOS transistors and providing an accurate voltage reference for low supply voltage operations. For such portable systems, power consumption reduction becomes essential to extend the battery lifetime and/or the communication range. This leads to a strong demand for circuit building blocks operating with low supply voltages and low power consumption. Among them, voltage reference circuits are ubiquitous; they are broadly used in analog and digital systems to generate a DC voltage independent of process, supply voltage and temperature variations.

IV Experimental Results:

	Bulk current generator	Current method trimming	Compensated sub threshold method
PROCESS	0.25 μ , CMOS	0.25 μ , CMOS	0.25 μ , CMOS
VDD	0.14V	0.14V-5V	0.14V-5V
Vref	320mV	320mV	320mV
power	25nW	14nW	9nW
Area	0.085 mm ²	0.0118 mm ²	0.035 mm ²

Conclusion:

The work of this paper is to design bulk driven and current trimming based sub threshold voltage reference circuit. This work is reducing the overall system power consumption level compare to existing methodology. A pure CMOS voltage reference based on sub-threshold technology is designed in this project. Two opposite temperature coefficient current which based on CMOS process sub-threshold region were created to add, in order to obtain low-temperature-drift voltage reference. At the same time, this achieves low power consumption, which is only 46.468 μ W. Unlike the other references, two different types of resistors were used in the design, which makes a low temperature coefficient: 16.33ppm/°C in the temperature range from -40 to 125 °C. The voltage reference is applicable to low-power and high-precision circuit systems.

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