ADVANCES in NATURAL and APPLIED SCIENCES

ISSN: 1995-0772
EISSN: 1998-1090
2016 April 10(4): pages 105-110

Published BY **AENSI Publication**
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Open Access Journal

Design and Performance Evaluation of Explicit Pulsed Register Element for Low Power VlSI Circuits

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Received 25 February 2016; Accepted 10 April 2016; Available 15 April 2016

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ABSTRACT

In this paper, a low power flip flop design featuring an explicit pulsed register element and also different types of modified explicit pulsed register element is presented. The clock to the modified latch is based on the signal feed through scheme is presented. The proposed modified design achieves better speed and power performance. The modified design also solves long discharging path problem. This explicit pulsed register element employs split path technique, n-mos logic and pseudo n-mos logic for further reduction in their switching activity and short circuit currents, respectively. Based on post layout simulation results using CMOS 0.12µm technology, the modified explicit pulsed register element achieves area saving up to and the power saving up to respectively. The MEPRE 3 achieves area saving up to 16.48% to 35.53% and the power saving up to 8.9% to 24.19% respectively.

KEYWORDS: CMOS, flip flop, low power, pulse triggered

INTRODUCTION

In recent trends the requirement of portable equipment is increasing rapidly so that development of VLSI design places a major role in the complex systems. Where all systems contain analog, digital as well as memory elements and all this can be integrated on a single chip for designing a circuit we come across many design metrics like low power, high speed and reduced area by considering these metrics. A novel of explicit pulse triggered flip flop is designed are extensively used as a basic, many type of flip flops are designed based on their operation like master and slave based flip flop, conventional transmission gate flip flop and pulse triggered flip flop is preferred compare with others because pulse triggered is one which can execute in a single stage instead of two stages and also sufficient latch narrow is present at the edge triggered flip flop. Pulse triggered flip flop is classified in to two types based on their pulse triggering , the pulse is triggered inside then it is implicit pulsed register element and if the pulse is triggered in explicit manner then it is explicit pulsed register element [12],[5],[1]. Here pulse generator is introduced for control of the pulse repletion rate frequency, pulse width and delay with respect to the internal or external trigger and high and low voltage of the pulses. It allow control over rise and fall time of the pulses. Fig 1 represents the block diagram of explicit pulsed register element.

To Cite This Article: P. Jeya Priyanka and Dr.K. Batri., Design and Performance Evaluation of Explicit Pulsed Register Element for Low Power VlSI Circuits, 2016. **Advances in Natural and Applied Sciences**. 10(4); Pages: 104-110

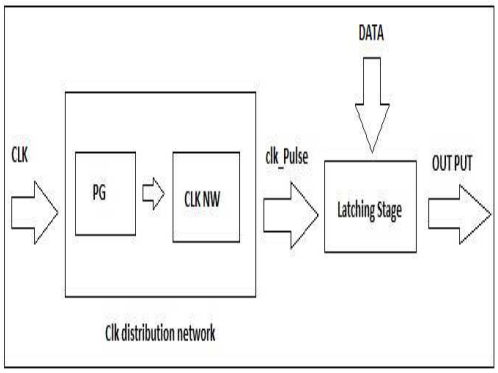

Fig. 1: Block diagram for the explicit pulsed register element.

Prpposed explicit pulsed register elements:

The Explicit Pulsed Register Element (EPRE) shown in fig(2) it has total number of 18 transistors including 12 clocked transistors and 6 unclocked transistors. In this module the latch part consists of 6 transistors namely MP1, MP2, MN1, MN2 and I1 respectively. The pulse generator is present at the starting point of the clock distribution network, the pulse generation circuitry is denoted as PG in fig(2,3,4,5) is made separately through two inverters and two input CMOS NAND gate. The clock pulses are diatributed from the clock distribution network to the latch part through the signal feed through scheme. This sharing helps in distributing the power of the pulse generator across many explicit flip flops. One input to the pulse generator NAND gate N1 is inverted and another one is normal and the output of the N1 is again inverted for further clock distribution network. When clock signal CLK changes from LOW to HIGH, then N1=1 and I3=0, MN3=0 then no clock signal is pulsed to the latch part. If the clock signals CLK changes from HIGH to LOW, then clock signal is pulsed. For further reduction of area and power we proposed a Modified Explicit Pulsed Register Element 1 (MEPRE1) shown in fig(3) it has total number of 17 transistors including 11 clocked transistors and 6 unclocked transistors. As compared with EPRE, the MEPRE1 have reduced interms of total number of transistors, area, power. Here feed forward technique is applied to the MP1 transistor and the clock pulses are given to the latch part through a signal feed through scheme. By analyzing this for small improvement in their performance we moved on to small modification, i.e., Modified Explicit Pulsed Register Element 2 (MEPRE2). The MEPRE 2 is shown in fig(4) it contains total number of 15 transistors including 9 clocked transistors. On comparing with EPRE and MEPRE 1, the proposed MEPRE 2 have reduced interms of total number of transistors, number of clocked transistors, area and power. Here Pseudo-nmos logic is applied to MP1 to reduce the internal discharge time. The gate terminal of MP1 is grounded therefore to get the MP1 transistor continuously remains in an on condition. The nmos logic is applied to the PN3 for further reduction. To get a power efficient register element on comparing with EPRE, MEPRE 1 and MEPRE we proposed the Modified Explicit Pulsed Register Element 3(MEPRE3) shown in fig(5). The MEPRE 3 contains total number of transistors 14 including 10 clocked transistors. The transistors are MP1, MP2, MN1, MN2, MN3, MN4, I1, I2 and N1. The input data is directly given to the transistors MP1 and MN3 at the time any one of the transistor remains on condition based up on the input HIGH or LOW. The nmos logic is applied to the transistor MN4 for further reduction. The clock pulses are given to the latch part through the signal feed through scheme.

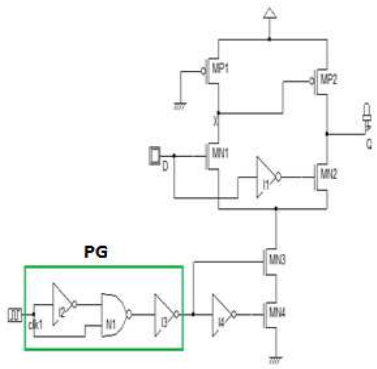

Fig. 2: EPRE (Total number of 18 transistors including 12 clocked transistors).

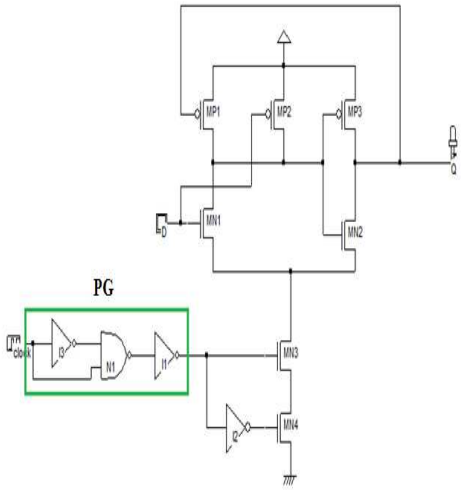

Fig. 3: MEPRE 1 (Total number of 17 transistors including 12 clocked transistors).

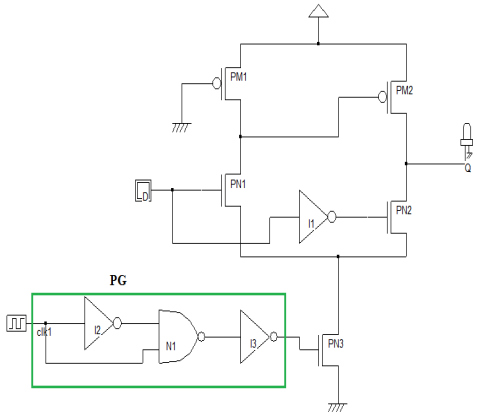

Fig. 4: MEPRE 2 (Total number of 15 transistors including 9 clocked transistors).

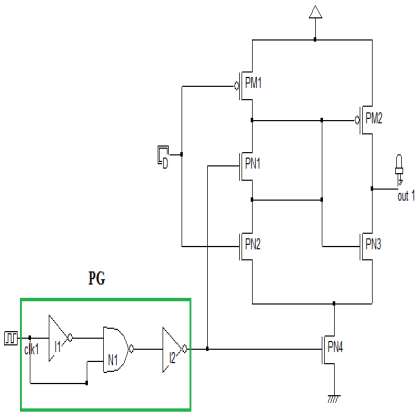

Fig. 5: MEPRE 3 (Total number of 14 transistors including 10 clocked transistors).

Simulation results and discussion:

The simulation results were obtained from DSCH & MICROWIND3.1 simulations in 0.12µm CMOS technology at room temperature Vdd is 1.8V. A clock frequency of 250 MHZ is used. Each design is simulated using the circuit at the layout level. Performance parameters such as area, power and delay are obtained by layout simulation. The Table I: shows the comparison of total number of transistors, total number of clocked transistors, area, power and delay between EPRE, MEPRE1, MEPRE2 and MEPRE3. Table II: shows the comparison of power delay product, energy delay product and power energy product for the same EPRE,

MEPRE1, MEPRE2 and MEPRE3. Table 1 shows the comparison between EPRE, MEPRE1, MEPRE2 and MEPRE3. In view of transistors the MEPRE3 uses less No. of transistors as compares with EPRE, MEPRE1 and MEPRE2. The area of MEPRE1 is 16.48% less compared to EPRE. The area of MEPRE2 is 25.27% less compared to EPRE. The area of MEPRE3 is 35.53% is increased compared to EPRE. As compared with EPRE our MEPRE1 reduces 8.95% of total power consumption. As compared with EPRE our MEPRE2 reduces 12.91% of total power consumption. As compared with EPRE our MEPRE3 reduces 24.19% of total power consumption. On the other side the delay is increased. The EPRE delayed in 10ns, MEPRE1 is delayed in 11ns, MEPRE2 is delayed in 12ns, and MEPRE3 is delayed in 14ns. Table II shows the comparison of MEPRE3 with EPRE, MEPRE1 and MEPRE2 in view of three matrices such as Power Delay Product (PDP), Energy Delay Product (EDP), and Power Energy Product (PEP) [8]. The conventional design metrics are to minimize the both power and delay product PDP. If D represents delay and P represents power consumption of the circuit then the metric can be expressed as PDP (energy) = Power (P)*Delay (D). It gives balanced geometric weights to power and delay. PDP optimizes both power and delay equally. EDP is another useful metric for evaluating the quality of the digital CMOS circuits design [3], expressed as EDP = Energy*Delay, EDP=P*D*D. But it may not be appropriate when the low power dissipation is priority. EDP gives a higher geometric weight to delay than the power. This metric is more suitable when the performance is the main concern. If the power is the higher priority than that the new metric power energy product PEP is considered both EDP and PDP matrices may not provide better solutions[2]. It gives higher geometric weight to power than delay and produces lower power solution than the other two matrices. It is expressed as

PEP = Power*Energy;

Fig (6) shows the layout design of EPRE, fig (7) shows the layout design of MEPRE 1, fig (8) shows the layout design of MEPRE 2, fig (9) shows the layout design of MEPRE 3 and fig (10, 11, 12) shows the comparison of total number of transistors used, total power consumption and total area required.

Table 1: Comparison of general parameters.

Register element name	No. of transistors	No. of clocked transistors	Area (μm^2)	D_Q Delay (ns)	Total power (μw)
EPRE	18	11	273	10	6.386
MEPRE1	17	8	228	11	5.814
MEPRE2	15	6	204	12	5.561
MEPRE3	14	6	176	14	4.847

Table 2: Comparison of Optimization parameters.

Register element	Power Delay Product (PDP)	Energy Delay Product (EDP)	Power Energy Product (PEP)
EPRE	$6.386*10^{-14}$	$6.386*10^{-22}$	$4.078*10^{-19}$
MEPRE1	$6.395*10^{-14}$	$7.034*10^{-22}$	$3.718*10^{-19}$
MEPRE2	$6.673*10^{-14}$	$8.007*10^{-22}$	$3.710*10^{-19}$
MEPRE3	$6.785*10^{-14}$	$9.500*10^{-22}$	$3.289*10^{-19}$

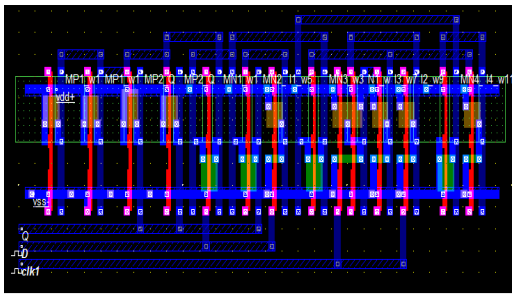

Fig. 6: Layout design of EPRE.

Conclusion:

In this brief, we presented a Modified Explicit Pulsed Register Element by employing a m0odification in Explicit Pulsed Register Element. The proposed Modified Explicit Pulse Register Element 3 employs Pseudo NMOS technique, Feed forward technique, NMOS logic and signal feed through scheme is used. The MEPRE 3 results in reduced short circuit power dissipation and switching activity. Finally, when the MEPRE 3 achieved area saving up to 16.48% to 35.53% and the power saving up to 8.9% to 24.19% respectively. In view of power consumption and area, this MEPRE 3 consumes less and outperforms prior arts in the EPRE design.

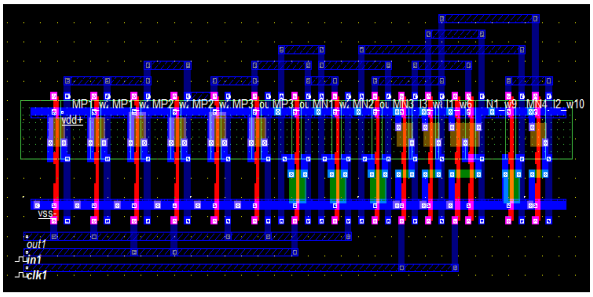

Fig. 7: Layout design of MEPRE1.

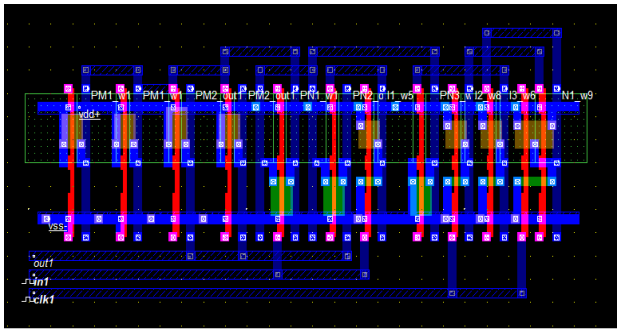

Fig. 8: Layout design of MEPRE2.

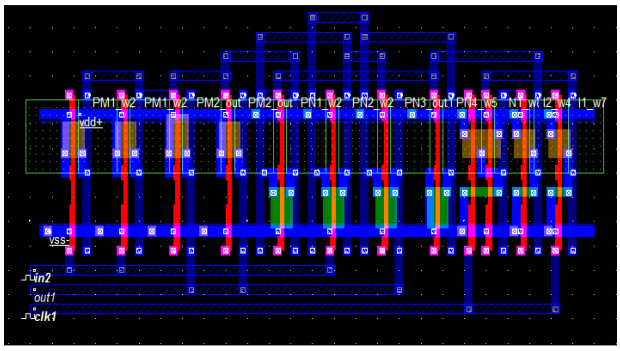

Fig. 9: Layout design of MEPRE 3.

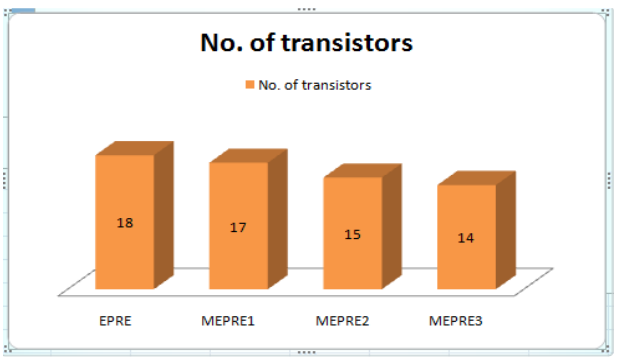

Fig. 10: Comparison of total number of transistors.

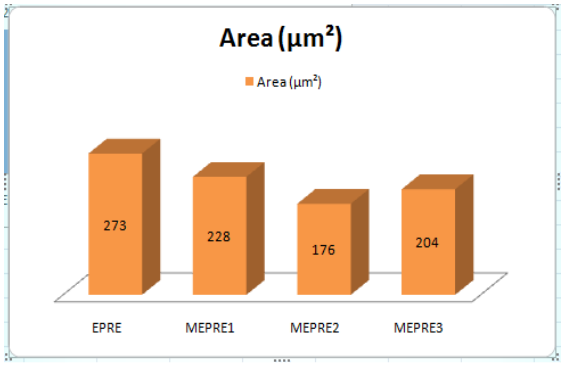

Fig. 11: Comparison of Area.

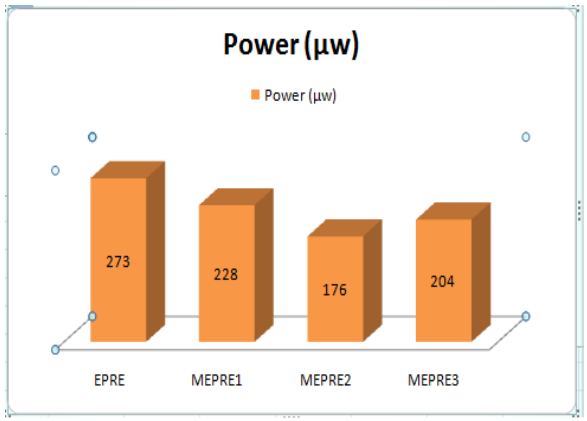

Fig. 12: Comparison of power consumption.

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