An Vlsi Architecture With Data Dependency Detector For Image Interpolation And Impulse Denoising

S. Arul Jothi, Dr. N. Santhiya Kumari and M. Ramkumar Raja

ECE Department, Sri Ramakrishna Engineering College, Coimbatore, Tamilnadu, India.

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ABSTRACT

Background/Objectives: Images captured by digital imaging devices are corrupted due to impulse noise during processing and storage. This image degradation has to overcome with low power device such as FPGA. Methods/Statistical analysis: The combined filters with T-model and inverse T-model convolution kernels are proposed for reducing the aliasing effect resulted by bilinear interpolation. Data dependency is proposed for VLSI implementation of a high performance processor with less memory requirement. Findings: A Novel method of data dependency has been used to design an area efficient VLSI Architecture for image interpolation algorithm. The blurring produced by the bilinear interpolation can be reduced by using a combined filter as pre-filter, the scaled image along with the impulse noise is send to the edge oriented filter and the noise is removed. The PSNR value of the scaled image after using combined filter is higher when compared with the PSNR value of the scaled image before using combined filter. The proposed method is a low cost, low complexity technique in terms of area, memory and power. The architecture takes a memory usage of 2MB less than the existing method, number of lookup table used is 168 which is 0.19% better than the existing method without data dependency, power is 0.23W less than the existing method.

Applications/Improvements: The computational complexity is less and hardware cost is low. It can be applied to digital imaging devices.

KEYWORDS: Digital imaging devices, FPGA, Combined filter, Data dependency, Interpolation

INTRODUCTION

Images could be processed in real time for some dedicated problems such as television standards conversion. Image scaling has been widely applied in the fields of digital imaging devices such as digital video recorders, high definition television, digital cameras, and mobile phones etc… images are corrupted by impulse noise during acquisition and transmission. Efficient denoising techniques are necessary to improve the performance of image processing methods. Jensen discussed about the nearest neighbor algorithm[1]. The non polynomial methods such as curvature interpolation[2] bilateral filter[3] and autoregressive model[4] are used for image zooming. Image processing algorithms with low complexity are necessary for VLSI implementation[5-8]. Various interpolation techniques are discussed in[9-13]. L.S.Usharani, P. Thiruvalar Selvan [14], et al presented a FPGA based impulse noise detection and correction method. John Moses C and Selvathi. D discussed about the area efficient VLSI architecture for image interpolation[15] Shih-Lun Chen and En-DiMa described about adaptive edge enhanced color interpolation processor.[16] Gour.P.N, Narumanchi.S, et al presented a real time image resizing using hardware accelerator.[17] Meng Li ,Peng Zhang,et al described about the VLSI implementation of edge directed video-up scalar using high level synthesis.[18]
This paper focuses only on the lower complexity techniques. The paper is organized as follows. In section II scaling and denoising algorithm is discussed. The improved VLSI architecture of the algorithm is described briefly in section III. The simulation results in section IV. Conclusion and future work in section V.

II. Proposed Scaling and Impulse Denoising Algorithm:

Figure 1 shows the block diagram of the scaling and impulse denoising algorithm. The scaling part consists of filters such as clamp, sharpening spatial filter, and bilinear interpolation. The denoising part consists of extreme data detector, edge oriented noise filter and impulse arbiter.

A. Sharpening Spatial filter:
Sharpening spatial filter is a type of high pass filter which is used to enhance the edges and the details of objects. It also removes the noise associated with the object.

B. Clamp Filter:
The unwanted edges are removed using a clamp filter which is a kind of low-pass filter. It also reduces the aliasing effects.

C. Bilinear Interpolation:
The principle behind the bilinear interpolation algorithm is to execute a linear interpolation in one direction, and then repeating the same in the all possible directions.

D. Simple Edge Preserved Denoising Technique [SEPD]:
This technique is used for removing fixed value impulse noise. In this paper a 3X3 mask W centering on P i,j is used for image denoising.

E. Extreme Data Detector:
The minimum and maximum luminance values (MINinW and MAX inW) is detected using extreme data detector.

F. Edge Oriented Noise Filter:
Twelve directional differences from D1 to D12 as shown in the figure 2 is considered to decide the edge of the image.

Fig. 1: Block diagram of the proposed scaling and impulse denoising algorithm.

Fig. 2: Twelve Directional Differences of SPED.
G. Impulse arbiter:
In the impulse arbiter the pixel $P_{i,j}$ is corrupted and then $f_{i,j}$ is equivalent to $\text{MIN}_W$ and $\text{MAX}_W$.

III. Proposed VLSI Architecture:

![Block Diagram of the real time scaling and denoising Processor.](image)

The Figure 3 shows the proposed VLSI architecture which contains line buffer, register bank, controller, data dependency detector, combined filter, bilinear interpolator and SEPD.

A. Line Buffer:
Even line buffer and odd line buffer are used for realizing three scanning lines used by SEPD. Pixels at even and odd rows are stored by even line buffer and odd line buffer respectively.

B. Register Bank:

![Architecture of register Bank.](image)

Figure 4 shows the register bank architecture. Three pixel values of a row in a mask are calculated using a three serially connected registers. The extreme data detector uses the nine values in the register to calculate the minimum and maximum value.

C. Data Dependency Detector:
To reduce the redundant computation in VLSI architecture, the data dependency detector reduces the redundant computations. This block try to explore the data dependency between the successive inputs, thereby reduces the unwanted computation.

D. Combined Filter:
The combined T-model and inversed T-model with a 3X3 convolution kernel. The sharpening spatial and clamp filter are realized using combined filter.
Fig. 5: Weights of the Convolution Kernels. (a) 3x3 Convolution Kernel. (b) Cross-Model Convolution Kernel. (c) T-model and Inversed T-model Convolution Kernels.

E. Bilinear Interpolator:
The output is calculated by the operations of the linear interpolation in both x- and y-directions with the four nearest neighbor pixels.

F. Controller:
Controller sends signals to control the pipelining operation and timing statuses of the combined filter.

G. Extreme Data Detector:

Figure 6 shows the architecture of the extreme data detector with three stage pipeline architecture. The output of the equality comparator EC will be one if the two inputs are same, then MininW and MaxinW values are calculated.

H. Edge oriented noise filter:
Figure 7 shows the two stage architecture of the edge oriented noise filter in which the SUB unit is used to calculate the difference between two inputs. The smallest directional difference Dmin is calculated using mintree.

I. Impulse Arbiter:
Figure 8 shows the Architecture of Impulse Arbiter. It is used to find whether the output of the filter is corrupted by noise or noise free. The comparator and the multiplexer is used to find the noisy pixel.

IV. Simulation Results:
A. Functionality Output:
The functionality verification as in Figure 9.1 and Figure 9.2 of the algorithm is done using MAT lab.
Fig. 7: Architecture of edge oriented noise filter.

Fig. 8: Architecture of Impulse Arbiter.

Fig. 9.1: Input Image
Fig. 9.2: Scale-down Image

B. HDL Designer Output:

The HDL designer outputs are obtained using modelsim simulator which is shown in the Figure 10 and Figure 11 and the comparison of PSNR which is obtained using MATLab is shown in the Table 1.
The performance comparison of various parameters with and without data dependency block is shown in the Table 2.

**Conclusion and Future Work:**
A low cost, low memory requirement, high quality and high performance VLSI architecture of the image scaling and impulse denoising processor with data dependency detector is proposed in this work. The experimental results shows that the blurring produced by the bilinear interpolation can be reduced by using a combined filter as prefilter. The scaled image along with the impulse noise is send to the edge oriented filter and the noise is removed. The PSNR value of the scaled image after using combined filter is higher when compared with the PSNR value of the scaled image before using combined filter. The proposed method is a low cost, low complexity technique in terms of area, memory and power. The architecture takes a memory usage of 2MB less than the existing method, number of lookup table used is 168 which is 0.19% better than the existing method without data dependency, power is 0.23W less than the existing method. The computational complexity is less and it can be applied to many real time applications as its hardware cost is low. As future work the architecture can be used for videos.

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<th>Parameter</th>
<th>Without Combined Filter</th>
<th>With Combined Filter</th>
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<tbody>
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<td>Input Image</td>
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<td>330 X 510</td>
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<td>Output Image</td>
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<td>18.0892 Db</td>
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<td>Scaling Factor</td>
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<table>
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<td>Power</td>
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<td>Number of LUTs</td>
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REFERENCES