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Design of a Dynamic 3 Bit Phase Shifter by RF CMOS Technology and Tunability with Neural Network

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ABSTRACT

In this paper we presented design of a dynamic 3 bit digital phase shifter . In all cases simulation obtained less than 1 percent error. We used a neural network with 2 inputs and 6 outputs, Inputs are central frequency and bit phase and outputs are bit elements. This network allows the designer, until we can design 6 bit phase shifter instead of central Frequencies around 2-4GHz;. In this design we used RF CMOS transistor for switching, we can design three phase shifter in 1.5-3.5GHz frequency range for each frequency. In other to we design dynamic new method for 6 bit phase shifter.

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INTRODUCTION

Phase shifter circuit apply in receiver and transmitter and pay attention to circuit operation in low frequency range (S-BAND frequency range) design of circuit can be have applications in wireless connection industrial, medical and science and applications in military radar and sweep array antenna . Figure 1 showed three phase shifter in receiving mode.

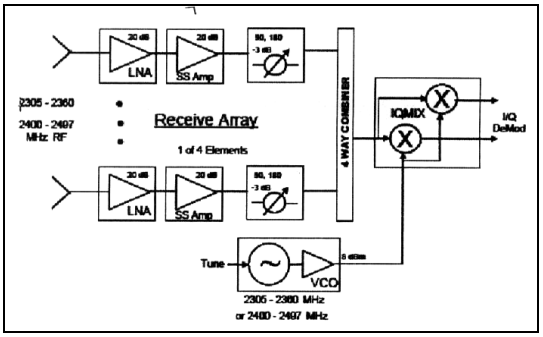

Fig. 1: Three phase shifter in receiving mode.

Three phase shifter apply in phase shift (-90, +90), (-45, +45), (-22.5, +22.5) and it can be secure phase sweep of -157, +157 degree. In one N bit phase shifter, every bit have one reference circuit and one delay circuit (figure 2), also every bit require 2 switch and 3 bit phase shifter require to 6 switch [2] .

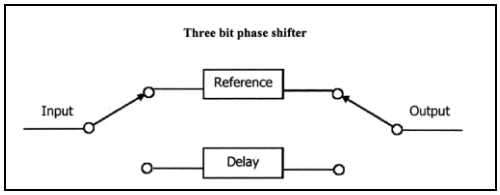

Fig. 2: Reference circuit and delay circuit

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Design method:

First, circuit design and simulated by ADS software and available almost in RF CMOS technology .it is important attend that for design one phase shifter or other delay circuit such as digital weekener or clock delay circuit we should remember that relative difference is very important between referenced and delay circuit for us and nothing .for example, when we design 90 degree phase shifter it isn't important that reference circuit should be product 0 degree phase and delay circuit produce 90 degree phase, perhaps, it is important for us that reference circuit phase minus delay circuit phase should equal 90 degree. In this paper, this subject expressed that design in delay and reference circuits is about 0 degree and it is easier relation to other modes .for example design +45 and -45 degree is easier than design 0, 90 degree that is for 90 degree phase shift. In this paper achieved phase (-90, +90), (-45, +45), (-22.5, +22.5) that are in range for phase differentiations 45, 90, 180 and finally these values deviate to rarely and these values was near to actual values .common topology showed in figure 3 for design phase shifter also for crating negative phase in one л network model that are of form one inductor and two capacitor and for crating positive phase used of л network model that is one capacitor and two inductor and in every two mode occupy area is rational on special layer.

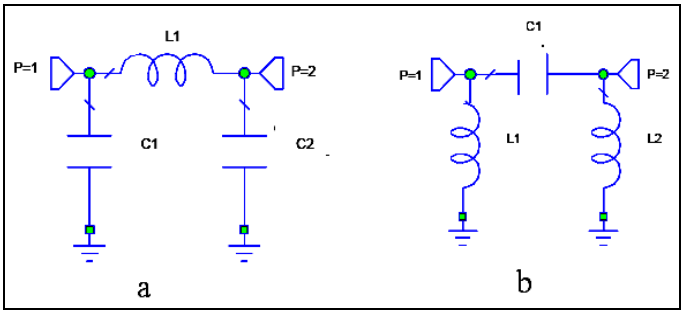

Fig. 3: Topology for crating negative phase and positive phase.

Diagram, block in figure 4, show one three bit phase shifter and in bit use two switch that we see them moving in near less values bit (22.5 degree) size of inductor and capacitor increase in positive phase and we solve this problem with using 45 degree positive phase and 22.5 degree negative phase and 22.5 degree positive phase will be achieve with accepted values.

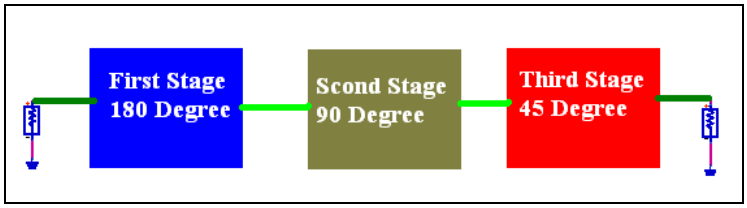

Fig. 4: Three phase shifter diagram block.

Switch

Primary applied topology for switch is parallel FET and series FET in way for switch by using parallel FET we can cause way for transfer signal to ground. Applied FET in this project is type of RF CMOS technology. We can use 24 transistors to design in this circuit [1], [7].

In this design switches should be operated according to that switch activation happens in positive phase when positive phase transistors have +5V, and negative phase transistors have -5V, and while negative phase activation, negative phase transistors have +5V and positive phase transistors have -5V. This operation cause one positive or negative phase in each step that we should pays attention to operation of transistors.

Theory of Shifters phase low-pass high-pass:

Introduced, they have transmission lines in their structures .These circuits have little length due to having high frequency but they don't cause problem: but when, we want design shift phase in lower frequency, due to having very much length in theist length in circuit dimension in Collecting, It isn't reasonable. The method introduced to design such a frequency is a method to use high-pass, low-pass circuits as it shown it Fig 5.

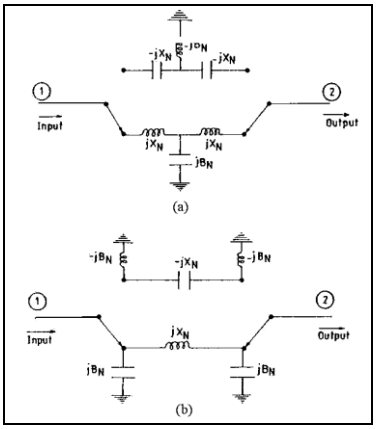

Fig. 5: Shifters phase low-pass high-pass (a) Type T (b) Type π

Since switch connect and place low pass mode, applied signal causes delay in phase and also when switch connect to mode of up pass, circuit causes a preference in phase and level of shift phase is developed by switching between these two models. Model T for circuit when connecting switch with low pass mode is as followed: coefficient of dispersion s21:

$$S_{21} = \frac{2}{2(1-B_N X_N) + j(B_N + 2X_N - B_N X_N{}^2)} \tag{1}$$

Where BN, and XN are normalized reactance and susceptance respectively. Created phase is:

$$\phi_1 = \tan^{-1}\left[-\frac{B_N + 2X_N - B_N X_N{}^2}{2\left(1-B_N X_N\right)}\right] \tag{2}$$

When switch connects with high pass mode, coefficient of dispersion S21 and level of phase ϕ_2 achieved by replacing -BN with XN in equation3.

$$\Delta\phi = \phi_1 - \phi_2 = 2\tan^{-1}\left[-\frac{B_N + 2X_N - B_N X_N^2}{2\left(1-B_N X_N\right)}\right] \tag{3}$$

It is assumed that there is no loss and we achieve perfect adoption conditions. Thus we have:

$$\left|S_{21}\right| = 1 \Rightarrow B_N = \frac{2X_N}{1+X_N^2} \tag{4}$$

With replacing this equation in equation 4. Difference of created phase achieved in equation 6.

$$\Delta\phi = 2\tan^{-1}\left(\frac{2X_N}{X_N^2 - 1}\right) \tag{5}$$

In expressed equations XN, BN Achieved In equation 6:

$$X_N = \tan\left(\frac{\Delta\phi}{4}\right) \tag{6}$$

$$B_N = \sin\left(\frac{\Delta\phi}{2}\right) \tag{7}$$

And we can say about circuit n in equation 8:

$$X_N = \sin\left(\frac{\Delta\phi}{2}\right) \tag{8}$$

$$B_N = \tan\left(\frac{\Delta\phi}{2}\right) \tag{9}$$

In such system, by increasing frequency, increasing phase delay is compensated by decreasing phase preference in high pass mode due to low pass mode. Therefore a fixed shift phase with coefficient of low VSWRS is created in a wide band. This kind of shift is the best kind of shift phase for UHF band. [5], [6].

Final Design circuit:

In figure 13, we see available design compose of three bits, this design in first bit is ±90 degree and second bit is± 45 degree and third bit is ±22.5 degree of phase shift and pay attention in to placing this step in three bit phase shifter with phase sweep of +157.5, -157.5, we cause turn on or off in positive and negative phase switch.

Pay attention to time limits, we cannot use of voltage reversions in the circuit cause easier operation therefore every bit of these circuits require to two control line with supplement voltage (-5, +5V) than can use for turn on and off in way of switch.

Simulation results with ADS2008:

The three bit phase shifter in 2-3GHz frequency rang described was in an RF CMOS technology and designed by ADS2008 with process having a supply voltage of ±5 V. A result simulation shows frequency rang 2-3GHz and center frequency 2.4 GHz.

Figures simulation of three bit phase shifter is shown in figure 6 and figure 7.

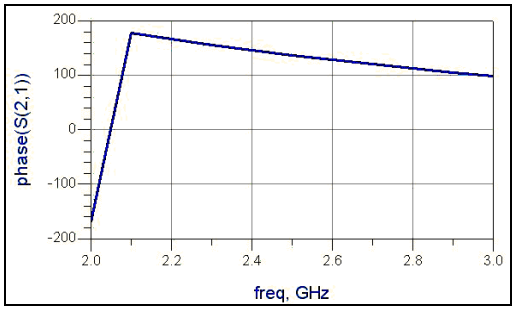

Fig. 6: Create phase at center frequency.

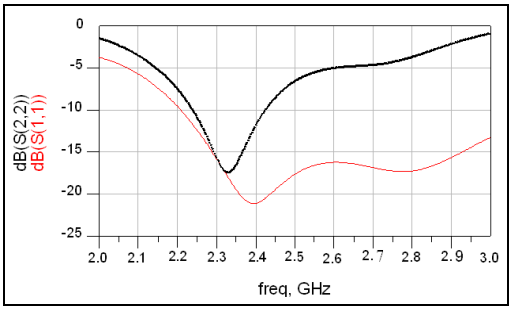

Fig. 7: Inputs and output impedance matching in center frequency.

Neural network:

*Structure**:***

In this step, we use a neural network with 2 input and 4 out put structure in order to design neural network. Inputs in these networks are desired central frequency (Frequency) used for design in phase shifter and bit phase count for obtaining elements of the same phase bit(Bit). (Frequency range is 2 to 3GHz and number 1 to 3 can be assigned to bit parameter. Number 1 is equal to bit phase 180 degree and number 2 is equal to bit phase 90 degree and number 3 is equivalent to bit phase 45 degree).

And outputs in this network show those capacitors of reference circuits and phase bit delays, L1, C1, L2, C2, Fig.8 shows this neural network. Structure of neural network has 3 layers so that it used in first layer design 2 neurons, in second layer 3 neurons and in third layer 4 neurons. And drive functions of first and second layers are

logarithmic sigmoid function ($f(n)=\frac{1}{1+e^{-n}}$)and range of drive function in third layer is (f (n) =n) linear function. [3], [4].

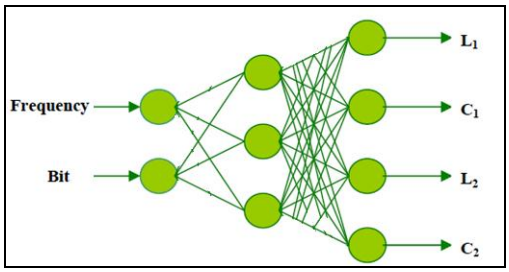

Fig. 8: Neural network diagram block used in design six bit phase shifter.

Result:

Instructing neural network and simulation error: In this part for instructing neural network we provided suitable values of self and reference circuit capacitors and all delays of bits for achieving desired phase shifts for per central frequencies frequency range of 2 to 3 GHz with step length of 20MHz. this accomplished by ADS software. After providing desired data we obtained 150 patterns, among these 129 patterns were used of neural network and 21 ones were selected for testing neural network. Finally after teaching neural network by using levenberg Marquardt algorithm and using 129 selected patterns, outputs (L1, C1, L2, C2) per 21 selected patterns was used as test data. We compared it with actual values of 21 test data. Figures 9-12 compare diagrams obtained by output of neural network per input test data and actual values of test data.

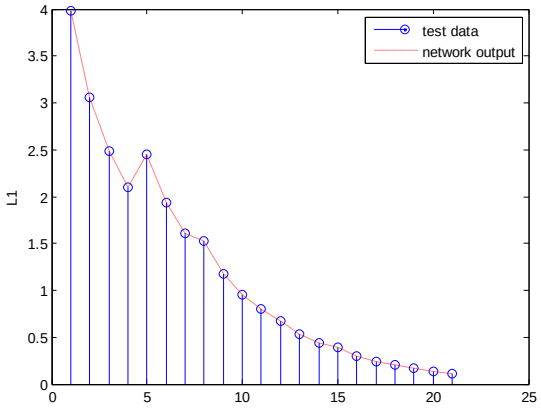

Fig. 9: Output curve neural network (L1) for input test data and out put test data curve.

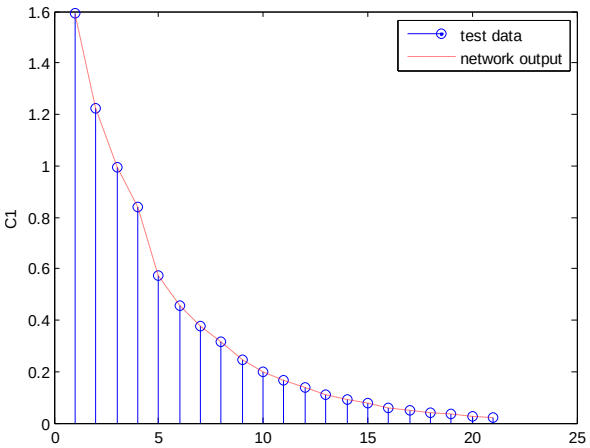

Fig. 10: Output curve neural network (C1) for input test data and out put test data curve.

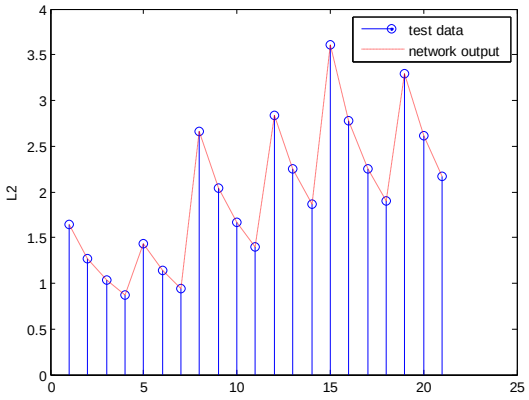

Fig. 11: output curve neural network (L2) for input test data and out put test data curve.

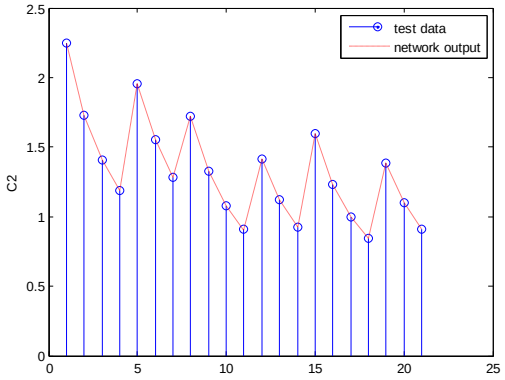

Fig. 12: Output curve neural network (C2) for input test data and out put test data curve.

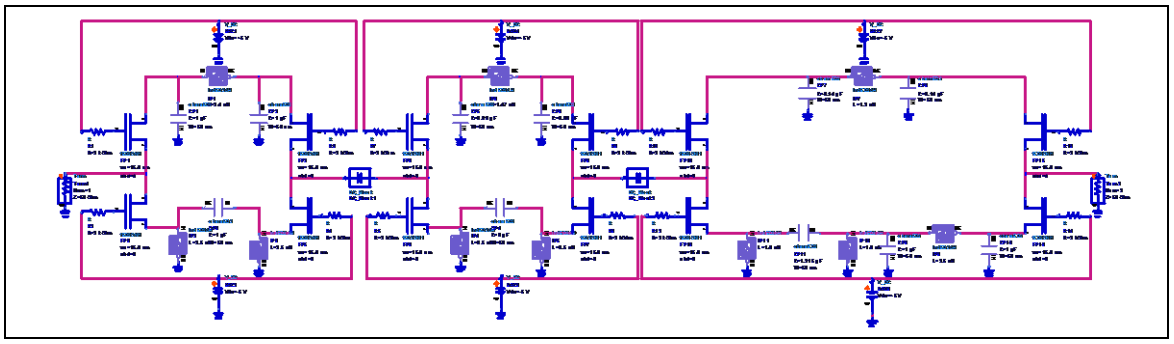

Fig. 13: Three phase shifter schematic.

Conclusion

In this Paper, the purpose is dynamic designing of a 3bit. As it can be seen in this paper we could design and simulate a phase shifter for central frequency of 2.4GHz using ADS software. This design consists of 3 classifications and in every class; there is a negative and a positive phase in each class. Then in order to achieve a dynamic design by using neural network we designed frequency 2-3 GHz .It means that we have the ability of designing any frequencies in this frequency range, we can achieve design of related element values by giving frequency and desired classification. That in these case values of elements was achieved with low errors respect to actual values by ADS software.

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